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Influence of Carrier Velocity Related Parameters on the Propagation Delay Time of CMIS Inverters with High-k Gate Dielectrics

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Abstract
It has been reported that the mobility (μ_{eff}) in MISFETs with high-k gate dielectrics is lower than that in the conventional MOSFETs [1,2]. We investigated the influence of carrier velocity related parameters (CVRP) on propagation delay time (τ_{pd}) of CMIS inverters. It is shown that τ_{pd} is strongly affected by shapes of mobility curves. This is explained by the fact that τ_{pd} is strongly affected by μ_{eff} in the high effective field (E_{eff}) region, around $V_G = V_{DD}$, and that μ_{eff} in the low E_{eff} region, around $V_G = V_{TH}$, and saturation velocity (V_{SAT}) have a relatively small influence on τ_{pd}. These observations are then explained based on physical considerations.

1. Introduction
The trend toward miniaturization has resulted in gate dielectrics being thinned, and it is estimated that they will soon be 1 nm for 35-nm MOSFETs [3]. In order to avoid the drastic leakage current increase that is inherent in SiO_2 gate dielectrics, high-k materials for gate dielectrics are being intensively investigated [4]. It has been reported that μ_{eff} in MISFETs with high-k gate dielectrics is lower than that in the conventional MOSFETs [1,2]. However, the E_{eff} region, in which the influence of μ_{eff} on τ_{pd} is the maximum, and the importance of the influence of V_{SAT} are not obvious. We therefore investigated the influences of these parameters on τ_{pd} using an in-house circuit simulator with a simplified transistor model and quantified each influence.

2. Model in Simulation
We used a transistor model based on the gradual channel approximation, taking the source/drain resistances into consideration. The effects of drain induced barrier lowering (DIBL), channel length modulation (CLM) [5-7], and velocity overshoot were also taken into consideration. Figure 1 shows the I_D-V_D characteristics of 50-nm gate length n- and p-MOSFETs with 1.3-nm-thick SiO_2 gate dielectrics. These characteristics agree well with those reported by Y.W.Kim et al [8]. Load capacitance was modeled by the sum of the junction capacitance at the bottom of the source/drain and the capacitances between the gate electrode and channel region and the source/drain, in which the Miller effect was considered. From the time dependences of the output voltages of CMIS inverters in a 7-stage ring oscillator (Fig. 2), τ_{pd} was calculated to be 2.36 ps. Here, the universal curve (UC) [9] was used for the mobility. This τ_{pd} is used as a reference value (τ_{pd0}). The design parameters for MISFETs in this and the following simulations are summarized in Table I. The influence of E_{eff} on μ_{eff} was modeled by the equation

$$\mu_{eff} = \mu_0/(1+\theta(V_G+V_{TH})) \text{ [10,11]}, \quad (1)$$

where μ_0 and θ were determined by fitting. Scattering by impurities in the substrate were not taken into consideration. The impurity profile in the channel region was uniform, and its concentration (N_{well}) was chosen so that short channel effects were sufficiently suppressed. Virtually, super steep retrograde profiles were assumed. An influence of neglecting scattering by impurities in substrates is quite small, as it will be shown in the section 4. V_{SAT} values were set 8×10^6 and 6×10^6 cm/s for electrons and holes (V_{SAT0}), respectively [7].

3. Simulations for High-k Gate Dielectric MISFETs
The mobility curves in the literature can be broadly classified into 2 groups (Fig. 3). Those in the first group are approximately equivalent to UC multiplied by a number less than 1 (type A), examples of which include the curves for ZrO_2/Si systems [1]. Those in the other group are almost independent of E_{eff} (type B), examples of which include the curves for in Al_2O_3/Si systems [2]. As for the other parameters, the values mentioned above were used. The results of a MISFET of L_G = 35 nm are summarized in Table II, which shows that τ_{pd} increases whenever μ_{eff} is degraded in the case of type A. In contrast, in the case of type B, τ_{pd} decreases for $\Delta\mu(V_{TH})$ = -30% or lower (not shown) in spite of the decrease in $\mu(V_{TH})$. This fact shows that τ_{pd} decreases when the amount of the decrease in $\mu(V_{TH})$ and the increase in $\mu(V_{DD})$ is comparable. τ_{pd} increases for $\Delta\mu(V_{TH})$ = -40%, however the amount of increase is quite small although the decrease in $\mu(V_{TH})$ is larger than the increase in $\mu(V_{DD})$.

4. Influences of Carrier Velocity Related Parameters on τ_{pd}
The μ_{eff} values at $V_G = V_{TH}$ ($\mu(V_{TH})$) and V_{DD} ($\mu(V_{DD})$) were changed to 0.7 or 1.5 times of the UC value and $\mu_{eff}(E_{eff})$ curves were generated tuning μ_0 and θ in (1) (Fig. 4). V_{SAT} was also changed to 0.7 or 1.5 times the reference value. In each simulation, only one of these 3 parameters was changed. Figure 5 shows the L_G dependence of the change in τ_{pd} induced by the changes of CVRP. It can be seen that the influence of $\mu(V_{DD})$ is the largest and that those of $\mu(V_{TH})$ and V_{SAT} are small. This is the reason for a decrease in τ_{pd} in the case of type B in spite of decrease in $\mu(V_{TH})$. It can also be seen that as L_G decreases, the influence of $\mu(V_{DD})$ decreases while those of V_{SAT} and $\mu(V_{TH})$ increase. Simulations changing other design parameters, such as X_j, $L_{overlap}$, $R_{S/D}$, $T_{G\text{-}ins}$, and V_{DD}, were also carried out and qualitatively equivalent results were obtained.
In order to study the effects of velocity overshoot, V_{SAT} was increased in the calculations of τ_{pd0}. The dependence of decrement in τ_{pd} for an inverter with L_G = 35 nm on V_{SAT} in τ_{pd0} calculation are shown in Fig. 6, which is induced by increasing CVRP to 1.5 times those in τ_{pd0} calculations. It can be seen that the influences of $\mu(V_{TH})$ and V_{SAT} are small for all the V_{SAT} values studied and that the influence of $\mu(V_{DD})$ is further increased by the velocity overshoot. However, the effect of velocity overshoot is not large.

5. Discussion
Figure 7 shows the current trajectory of an n-MISFET in the ring oscillator. It can be seen that only a small portion of the trajectory passes through the region where both V_G and V_D are low. Hence the influence of $\mu(V_{TH})$ on τ_{pd} is small. It can also be seen that a large portion of the trajectory passes through the region where the device operates in a saturation region. Hence, the influence of V_{SAT} appears to be the largest. However, this is not correct. When μ_{eff} is increased, the electric field strength, at which carrier velocity is equal to V_{SAT} (E_{SAT}), decreases. Hence, the drain saturation voltage ($V_{D,SAT}$) also decreases. This means that the increment of I_D due to CLM (ΔI_{CLM}) increases, i.e., I_D increases significantly (Fig. 8(a)). When V_{SAT} is increased, E_{SAT} and $V_{D,SAT}$ increase. This means that ΔI_{CLM} decreases, i.e., I_D increases only slightly (Fig. 8(b)). Hence, the influence of μ_{eff} on I_D is large while that of V_{SAT} is small, i.e., the influence of V_{SAT} on τ_{pd} is small compared with that of $\mu(V_{DD})$.
Next, the physical reasons for the L_G dependences of the influences are considered. As L_G decreases, the parallel electric field in the channel region increases. This means that the carrier velocity approaches V_{SAT}. Hence, the

influence of V_{SAT} increases and that of μ_{eff} decreases. The influence of $\mu(V_{TH})$ increases slightly in the short L_G region due to DIBL, because the phenomenon reduces E_{eff}. Hence, the degradation of μ_{eff} in low E_{eff} region should also be suppressed.

6. Summary and Conclusion

Our study showed that the influence of mobility in the high effective field region on τ_{pd} is quite large. Therefore, improvement of the quality of the interface between high-k gate dielectrics and the substrate is indispensable and an increase in carrier mobility, especially in high effective field region, is also essential.

Acknowledgements

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Table I Design parameters of the MISFETs used in the simulations.

	n-MISFET	p-MISFET
L_G	35 nm ~ 100 nm	
W_G	1.05 μm	1.75 μm
$T_{G\text{-}ins}$	5 nm	
$k_{G\text{-}ins}$	19.5	
X_j	10 nm	
$L_{overlap}$	7 nm	
N_{well}	2.5×10^{18} cm^{-3}	
$N_{S/D}$	1.0×10^{21} cm^{-3}	
R_c	3.0×10^{-8} Ωcm^2	
V_{TH}	0.1 V	- 0.1 V
V_{DD}	0.6 V	

Table II $\Delta\tau_{pd}$ values for the $\Delta\mu_{eff}$ values obtained in simulations with mobility curves of type A and type B in Fig. 3.

	$\Delta\mu(V_{TH})$	$\Delta\mu(V_{DD})$	$\Delta\tau_{pd}$
Type A ex. ZrO_2 [1]	- 10%	- 10%	+ 7%
	- 20%	- 20%	+17%
	- 30%	- 30%	+28%
	- 50%	- 50%	+65%
Type B ex. Al_2O_3 [2]	- 30%	+ 36%	- 8%
	- 40%	+ 17%	+ 2%
	- 50%	- 3%	+16%
	- 70%	- 42%	+69%

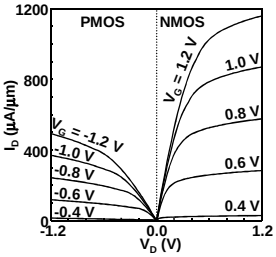

Fig.1 Simulated I_D-V_D characteristics of 50-nm gate length n- and p-MOSFETs with 1.3-nm-thick gate SiO_2.

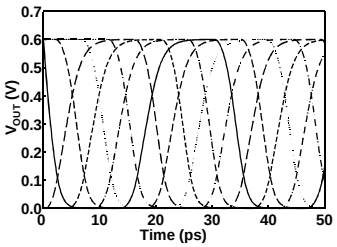

Fig.2 Time dependence of the output voltages of CMIS inverters in a ring oscillator.

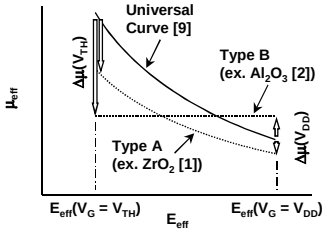

Fig.3 Schematic figure showing the 2 groups of reported mobility for MISFETs with high-k gate dielectrics.

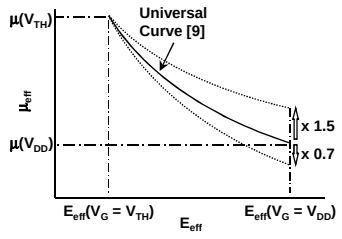

Fig.4 Schematic figure showing how to generate $\mu_{eff}(E_{eff})$ curves.

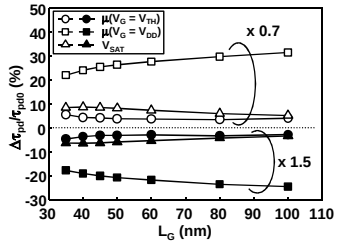

Fig.5 Gate length dependence of changes in τ_{pd} induced by changes in the velocity related parameters.

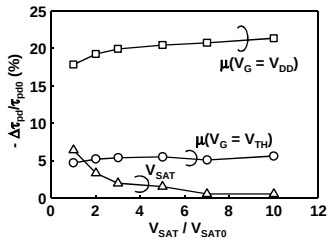

Fig.6 Dependence of the change in τ_{pd} on V_{SAT} for an inverter with L_G = 35 nm.

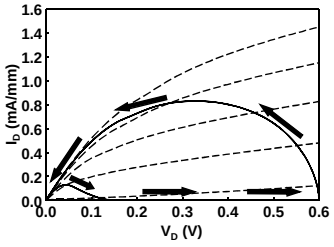

Fig.7 Current trajectory in an n-MISFET in a ring oscillator.

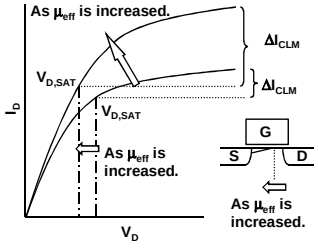

Fig. 8(a) Schematic figure of the changes when μ_{eff} is increased.

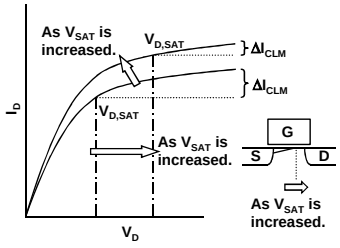

Fig. 8(b) Schematic figure of the changes when V_{SAT} is increased.