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Improvement of High-Speed Oxide-Confined Vertical-Cavity Surface-Emitting Lasers

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Introduction

The small volume of vertical-cavity surface-emitting lasers (VCSELs) resonators promotes high photon densities without excessive photon lifetimes and hence the potential for high speed operation, and are expected to be used with a high-frequency modulation over 10Gbps [1]. This inherent advantage makes VCSELs fit to be used as a light source in short-haul data-communication and high-speed optical interconnection.

Since RC time constant influence the modulation characteristics of VCSELs severely, great efforts had been done to minimize the resistance and the capacitance of the devices. Recently, most of the conventional high-speed VCSELs adopt ether intra-cavity / co-planar metal contact [2] or polyimide planarization [3] process to reduce series resistance and capacitance. But those approaches have many disadvantages and inconvenient for production [4].

To avoid these unfavorable process techniques, a simple method for high-speed oxide-confined VCSELs fabrication have already been demonstrated [4] [5]. The devices' static operation characteristics and lifetime test manifest the fabrication technology is adequate for mass production. But the high-speed dynamic performance seems not good enough for commercial application. In this report, an additional ion implantation procedure have been introduced into the process, and the eye-diagram now widely open up to 10Gbit/s.

1. Experiments

In this report, the oxide confined VCSEL epi-wafers were prepared by metal-organic vapor-phase epitaxy grown on n^+-GaAs substrate, whose structure consists of multiple quantum-wells GaAs active layer, sandwiched by fully doped n- and p-DBR mirrors. Both n- and p-DBR are composed of interlaced 1/4λ-thick $Al_{0.15}Ga_{0.85}As$ and $Al_{0.9}Ga_{0.1}As$ layers, and the periods are 39.5 and 22, respectively. The process procedure details were well described in previous work [4] [5]. And this time we adopt the same method to fabricate oxide-confined VCSELs, except the additional proton implantation for the purpose to reduce the parasitic capacitance. The mesa diameter of fabricated device is 22μm with a 5μm oxide aperture, and the device surface is quasi-planar so that the p-contact and the bondpad are on the same level. The p-contact was formed by directly depositing Ti/Pt/Au on the upmost heavily doped p^+ GaAs contact layer, and Au/Ge/Ni/Au was deposited on the bottom side of the substrate after thinned down, as revealed in Fig.1, and the shadow mark beneath bondpad denotes implanted region.

Neither intra-cavity / co-planar metal contact nor poly-imide resin planarization was used in the process.

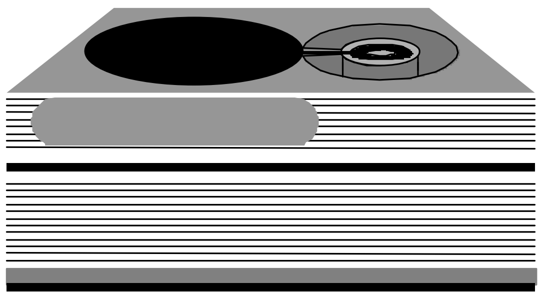

Fig. 1 Schematic illustration of proton implanted oxide-confined VCSELs.

After metal annealing, the sample was probe tested on wafer-level to extract static operation characteristics immediately, and subsequently been divided into two pieces. One of which was diced for package later, and the other was sent to take H^+ implantation with a dose of $10^{15}cm^{-2}$ for the purpose of further reducing parasitic capacitance. Preliminary we adopt four different proton energy ranges between 300 to 420keV according to the stopping and range of ions in matter (SRIM) simulation results, but the ideal combination of proton implantation energy in relative experiments are not optimized yet currently. The implantation region was kept away from the mesa to prevent damage from destroying the active region.

2. Results and Discussions

Fig. 2 shows the L-I-V characteristics of the fabricated VCSELs with (solid lines) and without (dash lines) proton implantation, respectively. The inset in lower right corner of Fig. 2 is a top view microphotograph of the emitting area.

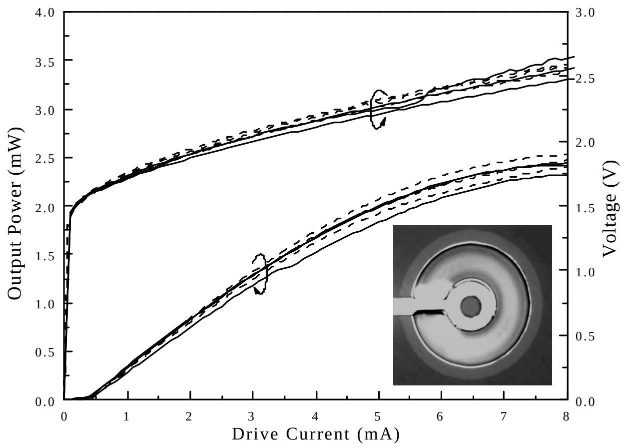

Fig. 2 L-I-V curves of three implanted devices (solid lines) and three devices without implantation (dash lines).

The L-I-V curves seem to be very similar before and after implantation. This result is quite different from previous report [6], because the mesas were entirely protected during implantation in this report and consequently no damage was introduced into the active region. Hence the threshold current can be maintained at the same value and DC characteristics aren't influenced. The threshold currents of both samples are 0.5mA and resistance are typically 90Ω.

The eye diagram of the device without implantation modulated at 10Gbit/s is shown in Fig. 3, the fall time tail slightly hit the mask obviously. And Fig. 4 reveals the eye diagram of the implanted device. Though the capacitance seems larger than other reports, the eye still widely open when modulate at 10Gbit/s. The rise and fall time of the implanted device are 44ps and 54ps, respectively.

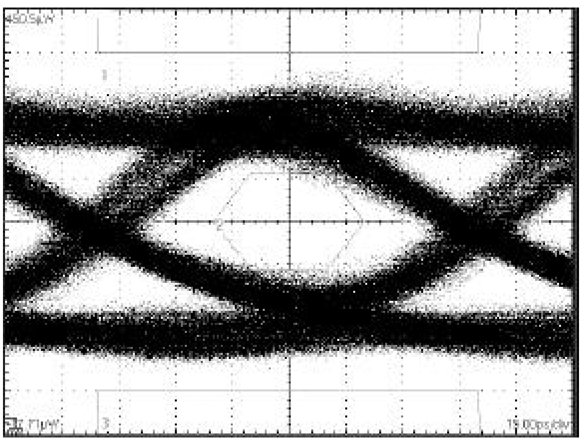

Fig. 3 Eye diagram of the device without ion implantation modulate at 10Gbit/s

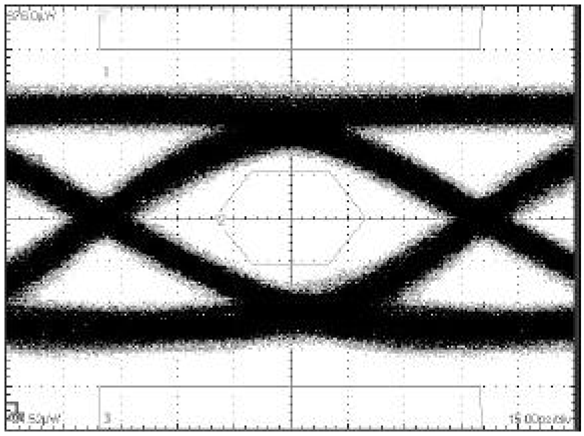

Fig. 4 Eye diagram of the device with ion implantation modulate at 10Gbit/s

3.Conclusions

High speed operating characteristics of oxide-confined VCSELs have been improved by using additional proton implantation. The eye diagram shows the devices can be modulated up to 10Gbit/s. And the L-I-V characteristics unaffected by implantation in this report.

Acknowledgements

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