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High- κ /Oxynitride Gate Dielectric - Searching for Serendipitous Materials -

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1. Introduction

The development of high- κ gate stacks, in which the gate length is less than 50 nm and the thickness is only a few nanometers, is the cutting-edge of material science and nanotechnology. It is particularly critical to integrate transition metal oxides (which need a high-temperature oxidation process) into sophisticated high-density devices. This is because a DRAM capacitor dielectric of Ta₂O₅ is the only successful application of the metal oxide in the past two decades with the exception of low-density FeRAMs. In this paper, we discuss the approach to developing high- κ gate materials.

2. Approach to material selection

Interface and degraded mobility

The oxide layer grown between the high- κ dielectric and the substrate was less focused on at the beginning of high- κ research in 2000 than it is today. This is because the growth of interfacial oxide was regarded as a negative effect for the exclusive purpose of reducing EOT. However, we realized that the interfacial oxide would eventually play a crucial role, similar to the interface of the Ta₂O₅ capacitor. We benchmarked the reported mobility against the thickness of the interfacial oxide and concluded that 2-nm-thick interface was required to attain electron mobility comparable to that of SiO₂ dielectric [1].

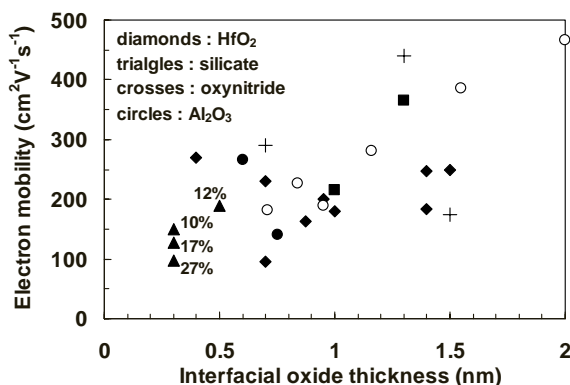


Fig. 1 Mobility benchmark. Mobility is defined by maximum values (solid). Triangles and open symbols denote silicates and our original data, respectively.

The mobility benchmark shown in Fig. 1 has been revised to include data newly reported in 2002 [2,3,6]. (The comparison was made semi-empirically, since the mobility was defined by a maximum value in a plot of mobility vs. electric field irrespective of dopant concentrations.)

Positive correlation is seen independent of what high- κ materials were applied.

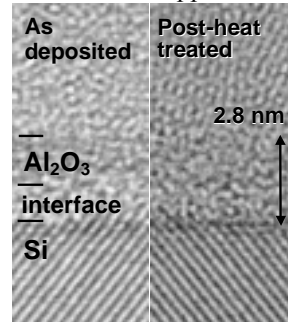


Fig. 2 Cross-sectional TEM view showing mixed interface.

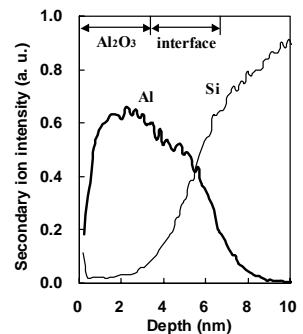


Fig. 3 Mutual diffusion of Al and Si at substrate interface.

We do not always adhere to a mechanism of remote-charge scattering due to a fixed charge which we believe to be the origin of the degraded mobility. Dopant diffusion from the substrate, inter-reaction, and local strain cannot be ruled out as multiple origins. In fact, when the post-heat treatment was done at temperatures above 1000°C, the Al₂O₃/SiO₂ interface became indistinguishable (Fig. 2), and the depth profile showed distinct mutual diffusions across the interface (Fig. 3). We think this mixed interface fluctuates the electric potential in the vicinity of the channel.

Inhomogeneous silicate

Non-uniform morphology is often seen in silicate dielectrics that are in a glassy state. However, the glass transition is the second-order transition accompanied by kinetics. Therefore, the crucial factors in the process are time and temperature. The quenching process produces a metastable and uniform amorphous dielectric. However, gradual heating and/or cooling relax the glassy film, change the volume, and may precipitate crystalline nano-spheres, because the chemical system is moving towards thermal equilibrium (depending on the chemical composition), especially near the glass transition temperature (800-600°C). The morphology of a Hf_{0.15}Si_{0.85}O₂ film that was deposited by sputtering and then post-heat treated in N₂ is shown in Fig. 4. Spherical particles are clearly visible, because their thickness was as large as 100 nm, and the film was post-heat treated above 1000°C.

The silicate dielectric is liable to phase-separate as the concentration of guest elements is increased. The significantly degraded mobility of silicate dielectrics (triangles) shown in Fig. 1, suggests that the gate dielectric consists of nano spheres dispersed throughout the silicate

glass. Taking account of a higher glass transition temperature and namely a stable amorphous state, aluminate is preferable to silicate.

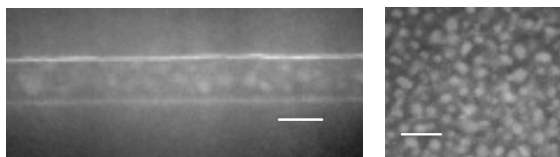


Fig. 4 Phase-separated Hf-silicate dielectric after high-temperature post-heat treatment (SEM photo, scale length = 100 nm).

Interfacial oxide and gate leakage current

How thick must the interfacial oxide layer be in order to suppress the interfacial reaction and to eliminate the effect on mobility? The chemical potential of oxygen ions is a guideline for estimating the oxide interface. The chemical potential is constant within a uniform oxide, but at the interface adjacent to a non-oxide layer, a concentration gradient, that is, a chemical potential gradient of oxygen ions will result. Therefore, the high- κ oxide should be adjacent to a different oxide, in this case the interfacial oxide, in order to minimize the oxygen deficiency at the interface. A typical transition layer between SiO_2 and Si is 0.5 nm thick, which results in a 0.5-to-1.0-nm transition layer, including the interfacial oxide at the high- κ /Si interface.

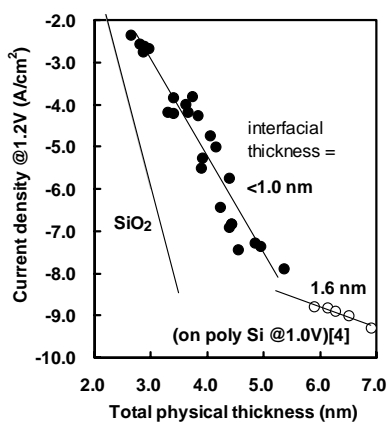


Fig. 5 Gate leakage current plotted against total thickness of high- κ dielectric and interfacial oxide.

The first objective of applying a high- κ dielectric is to thicken the gate dielectric layer and thus to reduce the gate leakage current. In Fig. 5, the leakage current is plotted against the total physical thickness of the Al_2O_3 dielectric and the interfacial oxide. Note that the leakage current is higher in the high- κ dielectric than in a conventional SiO_2 dielectric with the same total thickness. Decreasing the interfacial thickness from 1.6 to 1.0 nm [4] changes the slope of the thickness dependence and further increases the leakage current. We think that the resulting defective interface lowers the barrier height and increases the leakage current when the interfacial thickness is small. This will be proven if Fowler-Nordheim tunneling through interfacial SiO_2 became predominant, as seen in the Ta_2O_5 capacitor

[5]. The minimum thickness of the interfacial SiO_2 is approximately 1.5 nm while maintaining high mobility and low leakage.

Nitridation and nitrided interface

A high-temperature process may crystallize the amorphous film and provide filamentary leakage paths along the grain boundaries. Partially nitrided HfO_2 and Al_2O_3 [6] are thought to be analogous to oxynitride glass, which has glass-transition temperatures and crystallization temperatures higher than those of silicate glasses. Another approach is by surface and/or interface nitridation. We applied an interfacial SiON with an enriched oxygen concentration at the substrate interface (OI-SiN) [7] to the Al_2O_3 gate stack. The OI-SiN interface suppressed dopant diffusion (Fig. 6) and recovered mobility (Fig. 7). This is likely due to the effect of the increased physical thickness of the interface.

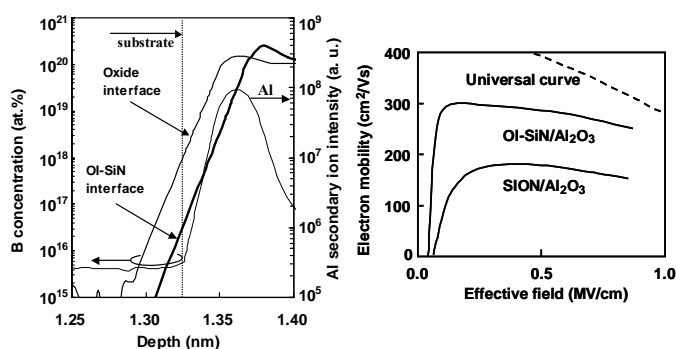


Fig. 6 Suppressed inter-diffusion via oxynitrided interface. Fig. 7 Mobility recovered in Al_2O_3 /SiON gate stack.

3. Conclusions

If we apply a simple combination of Al_2O_3 dielectric (1.5 nm) and an oxynitrided interface (1.5 nm) to conventional structures, the total thickness of 3.0 nm and EOT of 1.8 nm will enable low stand-by power applications. An alternative would be a nitrided aluminate having a higher κ . The serendipitous materials emerging from the above discussion are simple, although a variety of materials, structures and processes are currently being explored.

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