# Influence of Dielectric Constant Distribution in Stacked Gate Dielectrics on Electron Mobility in Inversion Layers

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## Abstract

In this paper it is shown that electron mobility in the inversion layer is strongly affected by the dielectric constant distribution in gate dielectrics. An explanation of this phenomenon based on physical considerations is provided using a simplified model. Preferable dielectric constant distributions for high mobility are discussed.

#### 1. Introduction

The trend toward miniaturization has resulted in gate dielectrics being thinned, and it is estimated that they will soon be 1 nm for 35-nm MOSFETs <sup>[1]</sup>. In order to avoid the drastic leakage current increase that is inherent in SiO<sub>2</sub> gate dielectrics, high-k materials for gate dielectrics are being intensively investigated <sup>[2]</sup>. It has been reported that mobility ( $\mu_{eff}$ ) in MISFETs with high-k gate dielectrics is lower than that in MOSFETs with SiO<sub>2</sub> gate dielectrics. This is thought to be because of the fixed charges within gate dielectrics and at interfaces between gate dielectrics and substrates; therefore, the fabrication of interfacial layers (ILs) at high-k film/substrate interfaces has been studied <sup>[3-5]</sup>. We investigated the influence of the dielectric constant distribution on the electron mobility determined by remote Coulomb scattering by fixed charge ( $\mu_{RCS}$ ) using numerical simulations and a physical model, and found that  $\mu_{RCS}$  is strongly affected by dielectric constant distributions in gate dielectrics.

## 2. Simulation and Results

Simulations of µRCS were carried out for the stacked gate dielectric structure shown in Fig.1. The simulation model uses a pseudo-2 dimensional approximation and takes the screening of electric potential by other electrons into consideration. Only the lowest sub-band is considered. The reported interfacial charge density ranges from the order of  $10^{11}$  to  $10^{13}$  cm<sup>-2</sup> <sup>[4,6,7]</sup>. In this study, fixed charges (1x10<sup>12</sup> cm<sup>-2</sup>) were located at the high-k layer/IL interface. The results were almost the same whether they were located at the interface or inside the high-k layer provided that the distance from the channel was the same. The dielectric constants of both the high-k layer ( $\epsilon_h$ ) and the IL ( $\epsilon_i$ ) were varied from 3.9 to 100. The dependences of  $\mu_{eff}$  and  $\mu_{RCS}$  on the inversion carrier density (N<sub>inv</sub>) with fixed  $\varepsilon_h$  are shown in Fig. 2 with  $\varepsilon_i$  as a parameter. Figure 2(a) shows that  $\mu_{eff}$  at N<sub>inv</sub> = 5x10<sup>12</sup> cm<sup>-2</sup> (carrier density around V<sub>G</sub> = V<sub>DD</sub> <sup>[8]</sup>) is about 10% lower than the corresponding universal curve (UC) value <sup>[9]</sup> in the case of  $\varepsilon_i$  = 15. Figure 2(b) shows that  $\mu_{RCS}$  increases with  $N_{inv}$  due to the decrease in the scattering cross section caused by the increase in the average electron energy as well as the increase in the electric field screening effect. Interestingly, it can be seen that as  $\epsilon_i$  increases,  $\mu_{eff}$  and  $\mu_{RCS}$  first decrease and that us of increases, pen and pros inst decrease and then increase for the entire  $N_{inv}$  region studied. The dependences of  $\mu_{RCS}$  on  $\epsilon_i$  and  $\epsilon_h$  are shown in Fig. 3 with  $N_{inv}$  as a parameter. Here,  $\mu_{RCS}$  at  $N_{inv} = 5 \times 10^{12}$ cm<sup>-2</sup> is divided by 5. Figure 3(a) shows that µRCS has a minimum at an  $\varepsilon_i$  value of about 15. Figure 3(b)

shows that  $\mu_{RCS}$  shows a similar dependence on  $\epsilon_h.$ However, the tendency is much weaker and  $\mu_{RCS}$  increases virtually monotonically with  $\epsilon_h.$ 

#### 3. Discussion

 $\mu_{RCS}$  is inversely proportional to scattering probability, which is proportional to the square of the electric potential within the Born approximation. A stacked gate dielectric structure with a fixed charge (Fig. 4) was studied. The electric potential induced by the charge in the substrate can be analytically calculated by Fourier transformation in the plane parallel to the substrate surface, and can be represented as the infinite series of exp(-qTj) (j = 1, 2...), where q is a wave number in the Fourier transformation. The most dominant term in the series reveals that the electric potential is equivalent to that of a charge at the same position with a magnitude given by (1), provided that the dielectric constant of all layers is  $\epsilon_{Si}$ .

$$\frac{2\varepsilon_{Si}}{\varepsilon_{Si}+\varepsilon_{1}}\frac{2\varepsilon_{1}}{\varepsilon_{1}+\varepsilon_{2}}\cdots\frac{2\varepsilon_{n-2}}{\varepsilon_{n-2}+\varepsilon_{n-1}}\frac{2\varepsilon_{n-1}}{\varepsilon_{n-1}+\varepsilon_{n}}Q.$$
 (1)

In the case of gate stacks as in Fig. 1,  $\mu_{RCS}$  is expected to be proportional to  $[\epsilon_i/((\epsilon_{Si}+\epsilon_i)(\epsilon_i+\epsilon_h))]^2$ , whose dependence on  $\epsilon_i$  when  $\epsilon_h$  is fixed is shown in Fig. 5(a) together with the dependence of  $\mu_{RCS}$  on  $\epsilon_i$ . The dependence qualitatively agrees:  $[\epsilon_i/((\epsilon_{Si}+\epsilon_i)(\epsilon_i+\epsilon_h))]^{-2}$  has minimum at  $\epsilon_i = (\epsilon_{Si} \ x \ \epsilon_h)^{1/2} = 15.2...$  When  $\epsilon_i$  is fixed,  $\mu_{RCS}$  is expected to be proportional to  $(\epsilon_i+\epsilon_h)^2$ , whose dependence on  $\epsilon_h$  is shown in Fig. 5(b) together with the dependence of  $\mu_{RCS}$  on  $\epsilon_h$ . The dependences qualitatively agree, except that  $(\epsilon_i+\epsilon_h)^2$  has no minimum. The reason for this disagreement is that the terms other than the most dominant one and the electric potential screening by other electrons were neglected.

### 4. Preferable Dielectric Constant Distribution

In the stacked gate dielectric structure in Fig.1, lower and higher  $\epsilon_i$  than ( $\epsilon_{Si} \times \epsilon_h$ )<sup>1/2</sup> is preferable from the viewpoint of scattering probability by fixed charges in the high-k layer and/or at the interface between the 2 layers. When HfO<sub>2</sub> ( $\epsilon_h$  = 19.5) high-k layer is used, [ $\epsilon_i/((\epsilon_{Si}+\epsilon_i)(\epsilon_i+\epsilon_h))$ ]<sup>2</sup> is about 8990 for an SiO<sub>2</sub> ( $\epsilon_i$  = 3.9) IL and 4750 for an Si<sub>3</sub>N<sub>4</sub> ( $\epsilon_i$  = 7.8) IL. Hence the  $\mu_{RCS}$  for SiO<sub>2</sub> ILs is expected to be almost double that for Si<sub>3</sub>N<sub>4</sub> ILs. Note that this has nothing to do with the amount of fixed charge in the film. This is the pure influence of the dielectric constant of the IL. Metal silicate layers, e.g. (HfO<sub>2</sub>)x(SiO<sub>2</sub>)<sub>1-x</sub>, at the interface between substrates and metal oxides, e.g. HfO<sub>2</sub>, may degrade  $\mu_{eff}$  because they can have a higher dielectric constant than Si<sub>3</sub>N<sub>4</sub> layers. Figure 6 shows the dependence of the available  $\epsilon_i$  range on fixed charge density when  $\mu_{eff}$  values higher than certain specified values are to be achieved with N<sub>inv</sub> =  $5x10^{12}$  cm<sup>-2</sup> and a fixed  $\epsilon_h$  of 19.5 in the case of SiO<sub>2</sub> ILs ( $\epsilon_i$  = 3.9), fixed charge density should be lower than 1.7x10<sup>12</sup> cm<sup>-2</sup> or 8.1x10<sup>11</sup> cm<sup>-2</sup> in order to realize  $\mu_{eff}$  higher than 90 or 95% of UC, respectively. It is

known from (1) that upper bound for allowable fixed charge density decreases as  $\epsilon_i$  increases, provided that  $\epsilon_i$  is lower than  $(\epsilon_{Si} \ge \epsilon_h)^{1/2}$ . Considering that  $\epsilon_i$  is lower than  $\epsilon_h$  in most cases, it is indispensable to suppress fixed charge density in order to realize high  $\mu_{eff}$  and thin equivalent oxide thickness at the same time.

As for  $\epsilon_h$ , higher values are preferable since  $\mu_{RCS}$ increases almost monotonically with  $\epsilon_h.$  It is known from (1) that the available range of  $\varepsilon_i$  widens/shrinks when  $\varepsilon_h$  is higher/lower than 19.5.

#### 5. Summary and Conclusion

Our study showed that electron mobility in stacked gate dielectric structures is strongly affected by the dielectric constant distribution in the gate dielectrics, that mobility is minimum when  $\varepsilon_i = (\varepsilon_h \mathbf{x} \varepsilon_{Si})^{1/2}$ , and that mobility increases almost monotonically with  $\epsilon_h$ .

Gate electrode (metal) High-k gate dielectric : D.C. =  $\varepsilon$ 3.5 nm Q(Interfacial charge) = 1 x 10<sup>12</sup> cm<sup>-2</sup> Interfacial layer: D.C. =  $\varepsilon_i$ 0.3 nm

Substrate: D.C. =  $\varepsilon_{si}$  = 11.9 Impurity concentration = 3 x 10<sup>17</sup> cm<sup>-3</sup>

gate Fig.1 Stacked dielectric structure used in the simulations.



Fig.2(a) Dependences of simulated  $\mu_{eff}$  on the inversion carrier density with  $\varepsilon_i$  as a parameter.  $\varepsilon_h$  is set to 19.5.



Fig.3(a) Dependences of  $\mu_{RCS}$  on  $\epsilon_i$ with  $N_{inv}$  as a parameter. Here,  $\mu_{RCS}$  at  $N_{inv} = 5 \times 10^{12}$  cm<sup>-2</sup> is divided by 5.  $\varepsilon_h$  is set to 19.5.



Fig.5(a) Dependences of  $[\epsilon_i/((\epsilon_{Si}+\epsilon_i)(\epsilon_i+\epsilon_h))]^{-2}$  and  $\mu_{RCS}$  on  $\epsilon_i$ with  $N_{inv}$  as a parameter.  $\epsilon_h$  is set to 19.5.



Fig.3(b) Dependences of  $\mu_{RCS}$  on  $\epsilon_h$ with  $\dot{N}_{inv}$  as a parameter. Here,  $\mu_{RCS}$  at  $N_{inv} = 5 \times 10^{12}$  cm<sup>-2</sup> is divided by 5.  $\varepsilon_i$  is set to 3.9.



Fig.5(b) Dependences of  $(\epsilon_i + \epsilon_h)^2$  and  $\mu_{RCS}$  on  $\epsilon_h$  with  $N_{inv}$  as a parameter.  $\epsilon_i$  is set to 3.9.

Therefore, control of the dielectric constant distribution in gate dielectrics is indispensable.

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Fig.2(b) Dependences of simulated  $\mu_{RCS}$  on the inversion carrier density with  $\varepsilon_i$  as a parameter.  $\varepsilon_h$  is set to 19.5.



gate dielectric Fig.4 Stacked structure with a fixed charge.



Fig.6 Dependence of available range of  $\varepsilon_i$  in gate stacks such as that shown in Fig. 1.