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Experimental Evidence of Gate-Induced Schottky Barrier Height Lowering due to Image Force in Gated Schottky Diodes

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Abstract

In this report, the Schottky barrier height, ϕ_B, around the gate edge of gated Schottky diodes is thoroughly investigated. As a result, it is demonstrated that the increase of the gate voltage, V_G, significantly lowers the Schottky barrier height. The ϕ_B lowering is evaluated to be 0.1 eV at the V_G of 5 V, which can be quantitatively explained in terms of image-force-induced lowering of the potential. The implication of the gate-voltage-induced ϕ_B lowering for the ϕ_B engineering of Schottky S/D MOSFETs is also discussed.

Introduction

Schottky source/drain MOSFETs are promising as high performance devices in deep sub-50-nm gate regime [1-6], because of their excellent junction abruptness and inherently low source/drain parasitic resistance. In the Schottky S/D MOSFETs, it is considered that Schottky barrier of a nano-scaled Schottky junction, which is formed between the source-side metal and the inversion layer, significantly lowers the driving capability. Nevertheless, the characteristics of the nano-scaled Schottky junction, particularly as a function of the gate voltage, have not been fully clarified nor systematically investigated yet.

In this report, the characteristics of a nano-scaled Schottky junction formed around the gate edge of gated Schottky diodes are investigated as a function of the gate voltage, V_G. As a result, it is demonstrated, for the first time, that the increase of the V_G significantly lowers the Schottky barrier height, which is attributable to the image-force lowering.

Experiments and Discussions

A. Extraction of nano-Schottky diode characteristics

Fig. 1 shows a schematic structure of our gated Schottky diode. A nano-Schottky diode is formed between the metal ($CoSi_2$) electrode and the accumulation layer. As shown in Fig. 1, the diode current I_D consists of **a)** diode current at V_G of 0V, I_b, which mainly pass through the bottom of the entire Schottky junction and **b)** current through the accumulation layer, I_{acc}, which is additional current to I_b at the positive V_G's. Therefore, the current through the gated nano-Schottky diode, I_{acc}, can be extracted as $I_{acc}=I_D-I_b$.

Fig. 2a shows I_D-V_D characteristics, namely the characteristics of the whole junction, for various V_G's. Fig. 2b shows the I_{acc}-V_D, namely nano-Schottky junction, characteristics. The excellent agreement of I_{acc} with I_D at lower V_G suggests the successful extraction of nano-Schottky diode characteristics.

B. Schottky barrier height of gated nano-Schottky diode

By using the above nano-Schottky characteristics, the Schottky barrier height, ϕ_B, of the gated nano-Schottky junction can be evaluated. However, it should be noted that the current through a Schottky diode consists of two components: **a)** a tunneling component with a slight temperature dependence (thermionic field emission) and **b)** a thermal component with a temperature dependence of exp(1/*T*) (thermionic emission). In order to accurately evaluate the ϕ_B, these two components should be distinguished from each other. Fig. 3 shows the Fowler-Nordheim plot of the current through gated nano-Schottky diode for various temperatures, indicating that, whereas at 150 K the field emission is the dominant transport mechanism, the thermionic emission is dominant at temperatures height than 200 K and at V_D's of less than 0.05 V. Thus, with paying attention to these conditions, ϕ_B can be accurately evaluated from the temperature dependence of the thermal component of I_{acc} by utilizing the Arrhenius plot. Fig. 4 shows the ϕ_B-V_G characteristics, indicating a clear ϕ_B lowering with an increase in V_G.

C. Image-force potential lowering

The ϕ_B lowering can be understood in terms of image-force-induced potential lowering (Fig. 5). The increase of V_G induces the surface carriers, which results in the increase of electric field, *F*, in Si at the nano-Schottky diode interface. Since the total potential barrier is expressed as the summation of the field potential and the image force potential, higher *F* at higher V_G results in the lower potential barrier. Fig. 6 shows calculated the total potential barrier height, ϕ_B^{eff}, as a function of carrier concentration for various initial Schottky barrier heights, ϕ_B^0. The agreement of the theoretical and experimental results indicates that the image-force-induced potential lowering is the origin of the observed ϕ_B lowering.

D. ϕ_B engineering for high performance Schottky MOSFETs

The observed gate-induced ϕ_B lowering should be considered, when designing device parameters of Schottky S/D MOSFETs. Fig. 7 shows the relationship between surface carrier concentration and ϕ_B^0 for various ϕ_B^{eff}. It should be noted that, in order to obtain high performance Schottky S/D MOSFETs, ϕ_B^{eff} should be comparable to the thermal energy, say less than 0.1 eV. From Fig. 7, it is suggested that Schottky S/D MOSFETs with source metal of 0.2-eV ϕ_B have the potential to show the competitive performance with conventional MOSFETs, because its Schottky barrier height is almost negligible due to the ϕ_B lowering under high V_G conditions.

Conclusion

Schottky barrier height, ϕ_B, around the gate edge of a gated Schottky diode is thoroughly investigated. As a result, it is demonstrated that the increase of V_G significantly lowers the Schottky barrier height. The ϕ_B lowering can be quantitatively explained in terms of the image-force-induced potential lowering. Based on the above results, it is concluded that Schottky S/D MOSFETs with source metal of 0.2-eV ϕ_B have the potential to show the competitive performance with conventional MOSFETs.

References

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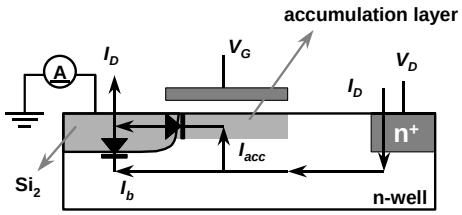

Fig. 1. Schematic of fabricated gated Schottky diode ($CoSi_2$/n-Si) and measurement setups. The thickness of the gate oxide was 10 nm. The channel length and width were designed to be 10 and 10 μm, respectively.

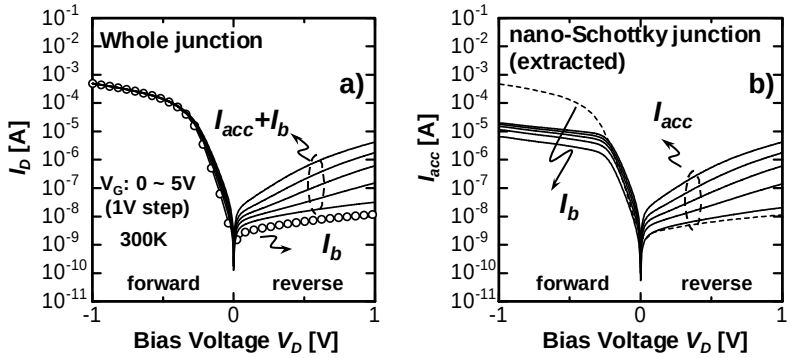

Fig. 2. Diode current versus diode bias voltage characteristics through **a)** a whole junction and **b)** a nano-Schottky junction of the gated Schottky diode as a function of V_G. The measurement temperature was 300K.

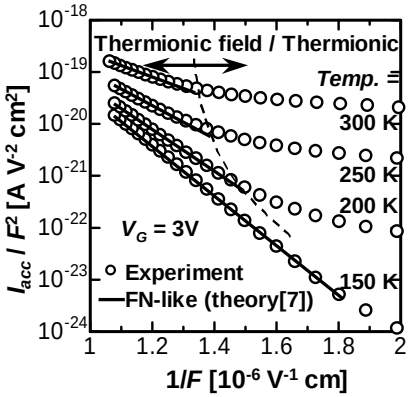

Fig. 3. Fowler-Nordheim plot of I_{acc}/F^2 as functions of $1/F$ for various temperatures at the V_G of 3V. The tunneling (thermionic field emission) components lie on the linear line

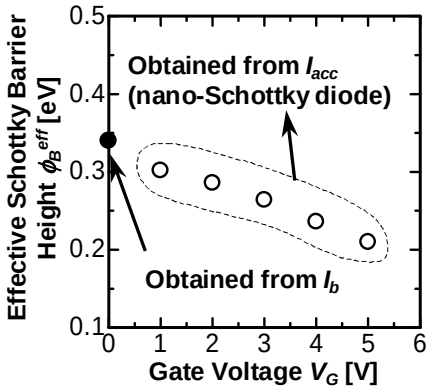

Fig. 4. ϕ_B versus V_G characteristics. The ϕ_B's are obtained by the Arrhenius plot of thermionic emission current. The ϕ_B lowering with an increase in V_G is clearly demonstrated.

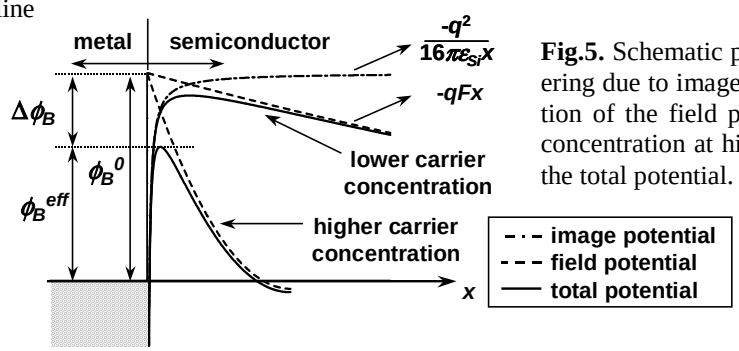

Fig.5. Schematic potential profile, illustrating the Schottky barrier lowering due to image potential. The total potential is given by the summation of the field potential and the image potential. The higher carrier concentration at higher V_G, resulting in the higher electric field, lowers the total potential.

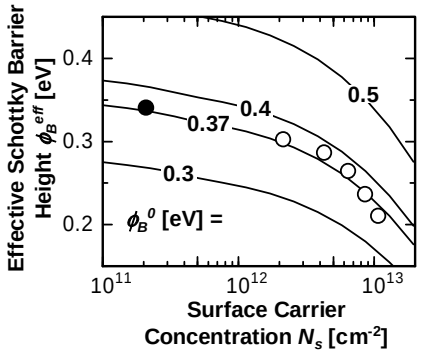

Fig. 6. Calculated and experimental Schottky barrier height, ϕ_b^{eff}, as a function of carrier concentration for various initial Schottky barrier height, ϕ_b^0. The meaning of the symbols is same as those in Fig. 4. The excellent agreement of theoretical and experimental results suggest that the experimentally observed ϕ_B lowering is due to the image-force lowering.

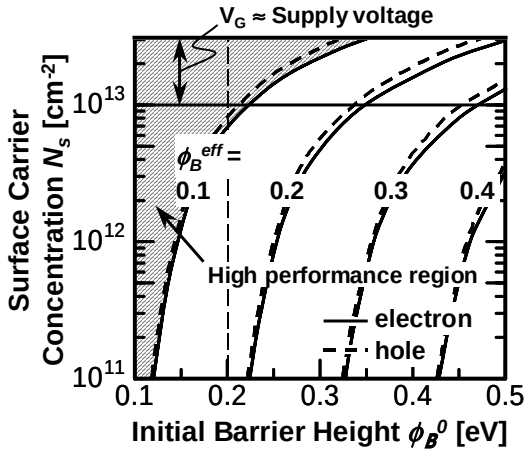

Fig. 7. The relationship between surface carrier concentration and ϕ_B^0 giving constant ϕ_B^{eff}'s. In order to obtain high performance Schottky S/D MOSFETs, ϕ_B^{eff} should be comparable to thermal energy, say less than 0.1 eV. The area satisfying this condition is indicated by the gray area.