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Intelligent BSIM4 Model Parameter Extraction for Sub-100 nm MOSFETs era

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1. Introduction

Compact models for CMOS devices and VLSI circuits have been widely studied in microelectronic industry over the past decades [1-3]. Among reported models, the BSIM3 and BSIM4 have been of great interest and played an important role between the semiconductor manufacturing companies and IC design houses. For the current sub-100 nm fabrication technology node, there are more than one hundred parameters to be extracted in the BSIM4 model. In deep-submicron MOSFET BSIM3 model parameter extraction, conventional statistic and local numerical methods, such as curve fitting, Newton iteration, and Levenberg-Marquardt (LM) minimization algorithms have been employed. These methods encountered several known deficiencies, such as (1) poor convergence without good initial guesses, (2) time-consuming for seeking optimal solution, (3) difficulty with simultaneous multiobjective optimizations, and (4) lack prediction capability for sub-100 nm MOFETs era. Furthermore, they also require a well-trained engineer with detailed knowledge of the MOSFET model and optimization methods to master the extraction process. With such local-method-based tools may increase the product manufacturing cost, prolong the time to market, and reduce the reliability.

In this paper an intelligent global methodology that automatically mimics engineer's extraction procedure is proposed. Based on: (i) the multiobjective distributed genetic algorithm (GA); (ii) the global monotone iterative (MI) based solution method; (iii) the automatic error tracking and inspection neural network (NN) scheme; and (iv) physical based empirical rules, this novel hybrid approach not only overcome those difficulties arisen from the conventional methods but also can extract more than 20 nanoscale transistos (90 nm NMOSFETs) in a global sense simultaneously.

2. Intelligent Extraction Methodology

It is known that the conventional parameters extraction procedure includes I-V curves measurement, model parameters extraction, and parameters verification, Fig. 1 shows the basic flowchart of the model parameters extraction architecture. Our intelligent extraction module includes data reduction, global MI-LM method, multiobject distributed GA, automatic inspection NN, and physical-based empirical rules. It extracts the model parameters automatically with right physical quantities in comparison with the measured data globally. Fig. 2 is a flowchart of the proposed intelligent parameter extraction technique. The GA extracting technique for HBT RF characterization and the MI for advanced deep-submicron device simulation have been developed in our recent work [4,5].

The data reduction is based on the model continuous property. Reduction of the massively measured data significantly reduces the computational complexity without losing the extraction accuracy. The intelligent extraction module then automatically extracts the BSIM4 model parameters for 90 nm MOSFETs from the sampled measured data. Our multiobject distributed GA bases on the mechanism of natural selection and natural genetics [4]. This simulation technique is with the global MI-LM method to compute the parameters and minimize errors [5]. It enables us to extract a lot of sets of I-V family curves at the same time. The errors of extracted parameters are controllable and less than 2.5% for all I-V curves and multi-transistors. Once optimal parameters are extracted (with global or local search), we apply the NN scheme which is trained to automatically detect and compare the measured and simulated curves, and therefore fine results can be obtained for any specific physical parameters.

3. Results and Discussion

With the developed extraction kernel, different technology nodes, such as 0.25, 0.18, 0.13 μm and 90 nm logic and analog devices have been verified. Tab. 1 reports the efficiency comparison with and without NN scheme for different sampling factors. The result suggests the sampling strategy reduces the time cost significantly. Tabs. 2 and 3 are the accuracy of the method. Important physical quantities V_{th} and Gm are extracted and compared with measured data in a reasonable range. More than 160 parameters in BSIM4 compact model for 90 nm technology, and we list some extracted parameters in Tab. 4. Fig. 3 is a score convergence comparison between w/ and w/o applying the smart NN scheme for the fine results inspection. It confirms the efficiency of the method. Fig. 4 suggests that the best performance at the population size 50. Figs. 5-8 demonstrate the evolution process for multiple 90 nm NMOSFETs (4 transistors are extracted simultaneously) I-V curves optimizations with our extraction kernel. We note here that the extraction procedures for nanoscale devices are achieved automatically.

4. Conclusions

In summary, an intelligent global methodology that automatically mimics expert extraction procedure has been proposed. It is based on: (i) the multiobjective distributed genetic algorithm (GA); (ii) the global monotone iterative (MI) based solution method; (iii) the automatic error tracking and inspection neural network (NN) scheme; and (iv) physical based empirical rules. This approach has successfully overcome some extraction difficulties in conventional methods. In our experience, it performed global parameter extraction within 2.5% accuracy for 20 nanoscale transistors (e.g., 90 nm N-MOSFETs).

Acknowledgements

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References

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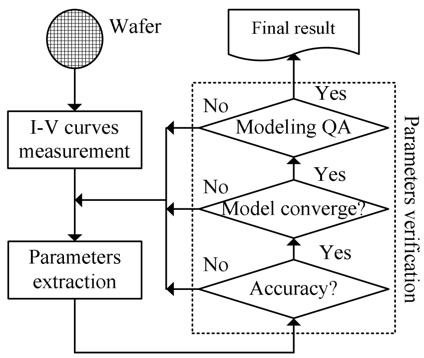

Fig. 1. A basic flowchart of model parameter extraction and optimization.

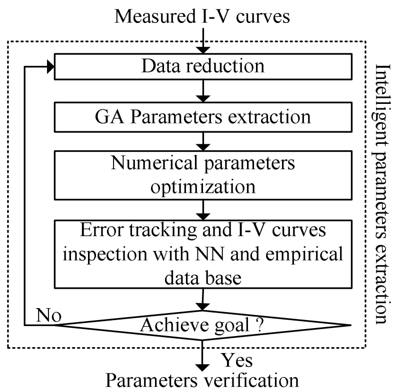

Fig. 2. A flowchart for our intelligent parameter extraction technique.

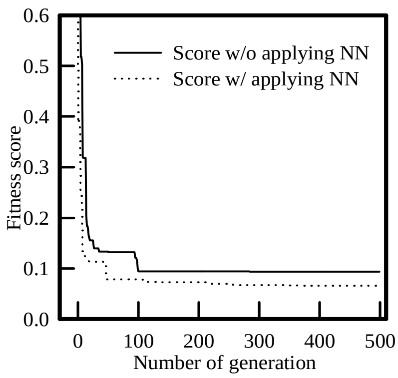

Fig. 3. A comparison of the extraction method w/ and w/o the automatic inspection scheme.

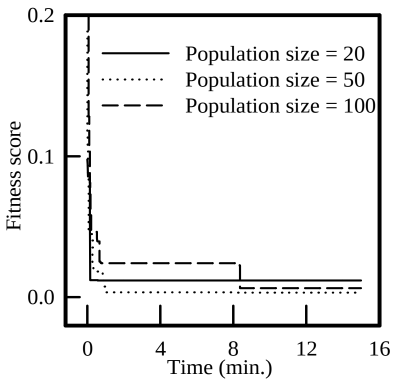

Fig. 4. A statistics of the population sizes effect in the nanodevice parameter extraction.

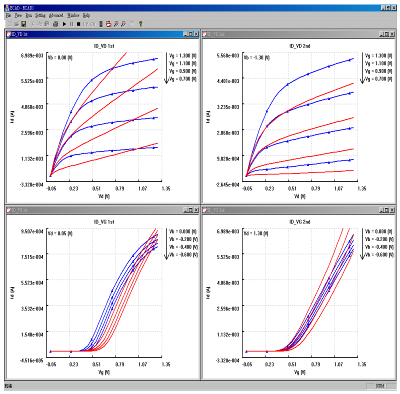

Fig. 5. The initial evolution. The blue dot-solid lines are the measured data to be extracted. The red solid lines are the extracted curves.

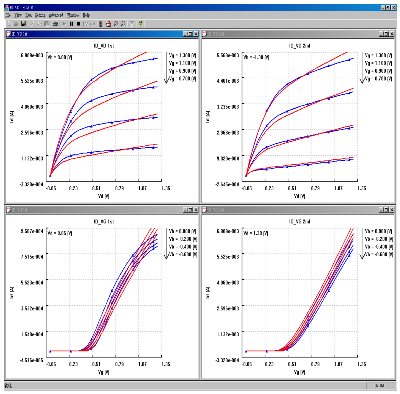

Fig. 6. The 30th evolution. The elapsed CPU time is 20 seconds.

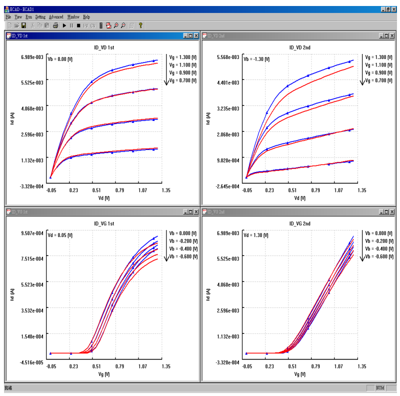

Fig. 7. The 300th evolution. The elapsed CPU time is 2.5 minutes.

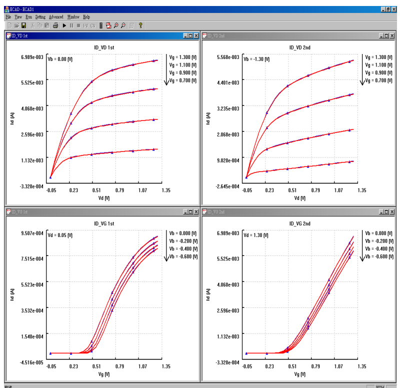

Fig. 8. The final extracted results (total generations are 387). The elapsed CPU time is 3.25 minutes.

Table 1. Data reduction strategy for the intelligent parameter w/ and w/o automatic error tracking and inspection scheme.

	CPU time.(sec)		I-V curves error (5000 generations)	
Sampling factor	w/o scheme	w/ scheme	w/o scheme	w/ scheme
1	5108	7189	0.037	0.007
3	2407	2899	0.022	0.010
5	1321	1724	0.019	0.010
10	655	905	0.029	0.012
20	361	762	0.041	0.012
30	192	390	0.052	0.014

Table 2. The measured and extracted V_{th} for NMOSFETs with different dimensions.

Length (μm)	Width (μm)	Measured Vth(V)	Simulated Vth(V)	Error (%)
0.09	0.09	0.4475	0.425	5.02
0.09	0.5	0.4472	0.435	2.72
0.09	1.0	0.4471	0.442	1.14
0.09	10	0.4465	0.441	1.23
0.13	0.09	0.4487	0.440	1.93
0.13	0.5	0.4485	0.439	2.11
0.13	1.0	0.4484	0.438	2.31
0.13	10	0.4480	0.441	1.56

Table 3. The measured and extracted Gm for NMOSFETs with different dimensions.

Length (μm)	Width (μm)	Measured GM(A/V)	Simulated GM(A/V)	Error (%)
0.09	0.09	3.19e-5	3.28e-5	2.77
0.09	0.5	9.33e-5	9.14e-5	2.08
0.09	1.0	1.72e-4	1.69e-4	1.74
0.09	10	1.58e-3	1.56e-3	1.27
0.13	0.09	1.94e-5	2.01e-5	3.22
0.13	0.5	6.29e-5	6.18e-5	1.86
0.13	1.0	1.19e-4	1.17e-4	1.68
0.13	10	1.12e-3	1.10e-3	1.31

Table 4. A list of extracted BSIM4 model parameters for 90 nm fabrication technology.

Name	Value	Name	Value
Vth0	0.3155	Vsat	101374
Vbm	-3	NFactor	1.18932
K1	0.4181	Cit	-2.58E-4
K2	-2.50E-2	Cdsc	2.47E-3
Eta0	7.16E-2	Cdscb	1.2E-4
Dsub	0.3790	Cdscd	0
U0	3.26E-2	Rdsw	72.9541
Ua	-1.16E-9	Drout	0.84
Ub	2.57E-18	Voff	-0.0942
Uc	8.35E-11	Wr	0.9442