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Channel direction impact of (110) surface Si substrate on performance improvement in sub-100 nm MOSFETs

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1. Introduction

Recently, performance improvement of MOSFETs by simple scaling approaches its limit and mobility enhancement technologies such as strained-Si channel [1] or control of surface orientation of Si substrate [2][3] are remarkably investigated. Use of different surface orientation such as (110) substrate is attractive from the viewpoint of conservative manufacturing processes without any unaccustomed materials such as SiGe [1]. However, a quantitative benefit of mobility enhancement to short channel characteristics has not been clarified yet. Moreover, crystal orientation along MOSFET channel should be optimized considering CMOS performance improvement.

We fabricated MOSFETs with various channel directions on (110) surface Si substrate with emphasis on fair evaluation of short channel performance through precise control of surface roughness and impurity profile. Precise carrier transport simulations were also carried out. And we discuss mobility enhancement and its benefit for CMOS performance improvement in sub-100nm regime.

2. Experimental condition and Simulation method

The MOSFETs were fabricated on (110) or (100) surface Si substrate based on 130 nm CMOS technology [4]. Six kinds of channel direction (<1$\bar{1}$0>, <001>, <1$\bar{1}$2>, <1$\bar{1}\bar{2}$>, <1$\bar{1}$1> and <1$\bar{1}\bar{1}$>) were prepared for (110) substrate. The gate oxide thickness was 2.0 nm for both (110) and (100) substrates by adjusting oxidation time. No other process change was made for (110) substrate. Physical gate lengths were down to 50 nm.

Electron and hole transport characteristics were calculated considering silicon full-band structure and involving phonon, impurity, and surface roughness scattering mechanisms. The same parameters were used for (110) and (100) substrate except for surface orientation parameters [5].

3. Results and Discussion

Channel direction dependence of mobility

Fig. 1 shows measured mobility in each channel direction on (110) substrate. Mobility improvement ratio ($\mu_{(110)}/\mu_{(100)}$) for nMOS (electron) and pMOS (hole) is about 30-40 % and 160-250 %, respectively. Furthermore, $\mu_{(110)}/\mu_{(100)}$ at high vertical field (E_{eff} >1 MV/cm), where surface roughness is dominant, is almost the same as that at low vertical field. Fig. 2 shows TEM images of poly-Si/SiO_2/Si structures in MOSFETs on (100) and (110) substrates. No clear difference in roughness is observed between the SiO_2/Si(110) and SiO_2/Si(100) intefaces. Therefore, $\mu_{(110)}/\mu_{(100)}$ does not change at high field region. Fig. 3 shows mobility improvement ratio in each channel direction (experiment and simulation). Simulation results reproduce experimental results well about the channel direction dependence without any parameter fitting. It is found that this dependence comes from anisotropicity of band structures.

MOSFET performance at sub-100 nm regime

Regarding ion implantation process, (110) axial channeling tends to give deeper penetration depth than (100) axial channeling [6]. Therefore, suppression of channeling is a key issue to downsizing (110) MOSFET. Fig. 4 shows SD extension depth-profiles on (110) substrate obtained from Monte Carlo ion implantation process simulation. These simulation results indicate that the halo implantation processes prior to the extension implantation give rise to efficient amorphization that can prevent undesired channeling effects for subsequent incident ions. Fig. 5 shows measured V_{th} lowering behavior ($|V_d|$=1.2 V) on (100) and (110) substrates. The same L_{min} for (110) and (100) regardless of channel direction is obtained as predicted by our process simulation.

Fig. 6 shows measured I_{on}-I_{off} characteristics ($|V_d|$=1.2 V) on (100) and (110) substrates. I_{on} of nMOS and pMOS on (110) substrate is about 65-75 % and 115-125 % of (100) substrate at I_{off}=100 nA/μm (L_g^n~65 nm and L_g^p~100 nm), respectively. The difference of I_{on} between (100) and (110) substrates is smaller than that of low field mobility due to high field transport effect. Table I shows propagation delay CV/I and on-current ratio I_{on}^n/I_{on}^p for various combinations of channel directions and surface orientations. Using the same channel direction at nMOS and pMOS on (110) substrate, CV/I is almost the same as that of (100) substrate. However, using the optimized combination of channel directions (<001> at nMOS and <1$\bar{1}$0> at pMOS), CV/I is improved by 5 %. Furthermore, asymmetrical I_{on} values for nMOS and pMOS can be improved from 2.45 for (100) case to 1.47 for the optimized combination. Further performance improvement can be possible with saving nMOS I_{on} degradation by using (110) surface for pMOS and (100) for nMOS.

4. Conclusions

Low field mobility and short channel characteristics on (110) surface Si substrate with various channel directions are investigated. $\mu_{(110)}/\mu_{(100)}$ does not depend on vertical field due to the same surface roughness for (110) and (100) substrates. Mobility enhancement and its channel direction dependence was verified by detailed carrier transport simulation. Good V_{th} lowering characteristics are obtained due to the suppression of channeling at SD extension by implant sequence control. CV/I and I_{on}^n/I_{on}^p improves using optimized combination of channel directions and (110) surface Si substrate is attractive for future LSIs down to sub-100 nm regime.

Acknowledgements

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References

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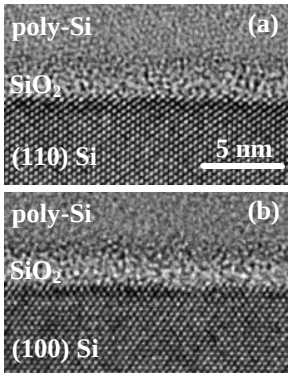

Fig. 2: Cross-sectional views of poly-Si/SiO_2/Si structures in MOSFETs on (100) and (110) substrates. (a) (110), (b) (100) substrate.

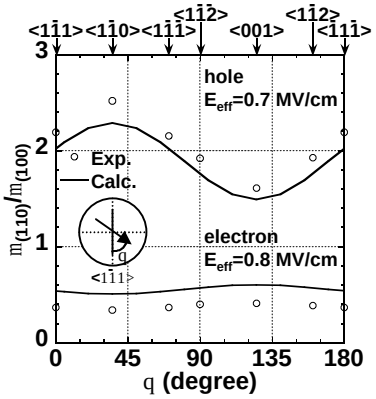

Fig. 3: Mobility improvement ratio in each channel direction on (110) substrate. Open circles indicate experimental results and solid lines indicate simulation results.

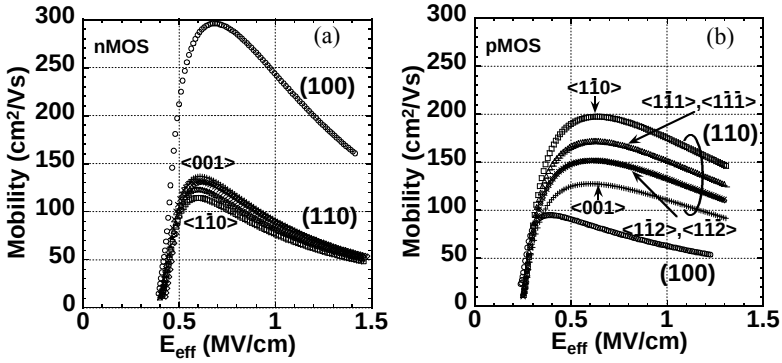

Fig. 1: Measured mobility in each channel direction on (110) substrate. Effective field is defined as $E_{eff}=(Q_{dpl}+Q_{inv}/2)/\varepsilon_{si}$ for both (100) and (110) MOSFETs where Q_{dpl} is the depletion layer charge density and Q_{inv} is the inversion layer charge density. (a) N-MOSFETs, (b) P-MOSFETs.

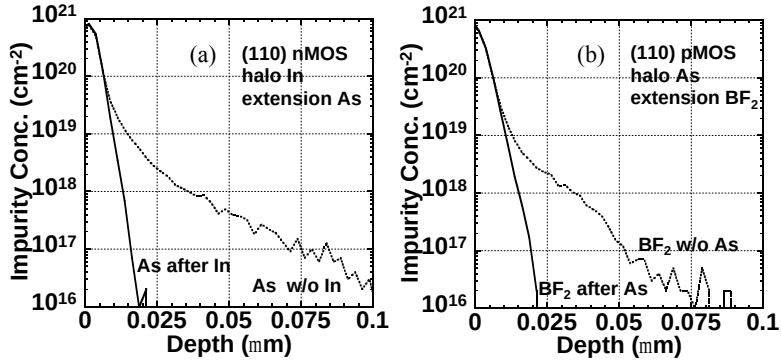

Fig. 4: SD extension depth-profiles on (110) substrate obtained from Monte Carlo ion implantation process simulation. (a) As (nMOS), (b) BF_2 (pMOS). SD extension implantation was carried out after halo implantation in order to suppress the channeling of extension ion on (110) substrate.

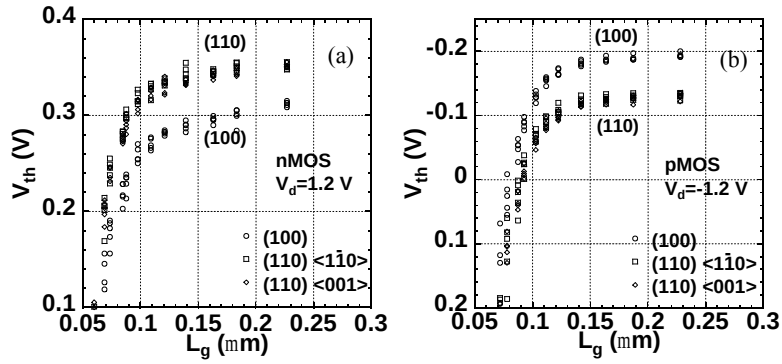

Fig. 5: Measured V_{th} lowering behavior in saturation region ($|V_d|$=1.2 V) on (100) and (110) substrates. (a) N-MOSFETs, (b) P-MOSFETs.

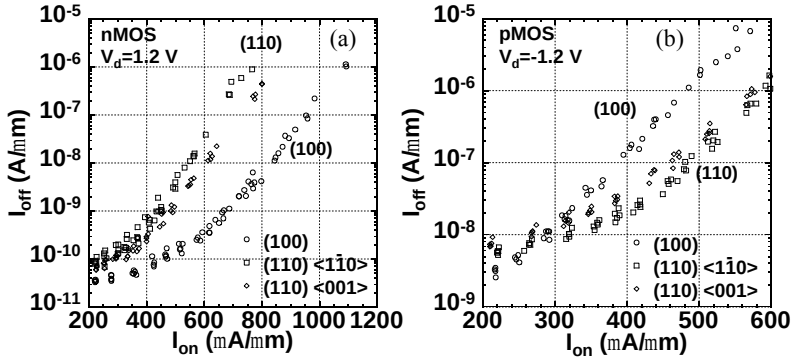

Fig. 6: Measured I_{on}-I_{off} characteristics ($|V_d|$=1.2 V) on (100) and (110) substrates. (a) N-MOSFETs, (b) P-MOSFETs.

Table I: Propagation delay CV/I (normalized by (100) value) and on-current ratio I_{on}^n/I_{on}^p for various combinations of channel directions and surface orientations. I_{off}=100 nA/μm and gate length of nMOS and pMOS is ~65 nm and ~100 nm, respectively. Optimized combination of channel directions on (110) substrate is <001> at nMOS and <1̄10> at pMOS.

	(100)	(110)			(100):nMOS (110):pMOS
nMOS	<1̄10>	<1̄10>	<001>	<001>	<1̄10>
pMOS	<1̄10>	<1̄10>	<001>	<1̄10>	<1̄10>
Normalized CV/I	1.0	1.01	0.99	0.95	0.85
I_{on}^n/I_{on}^p	2.45	1.28	1.57	1.47	1.95