Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 722-723

A-9-4

High Performance Strained Si/SiGe N-channel MOSFETs: Impact of Alloy Composition and Layer Architecture

SH Olsen, LS Driscoll, KSK Kwa, S Chattopadhay, AG O'Neill

School of Electrical, Electronic and Computer Engineering, University of Newcastle, U.K.
Phone: +44-(0)191-280-4310 E-mail: sarah.olsen@ncl.ac.uk

Abstract

Single and dual n-channel strained Si MOSFETs, fabricated by the same high thermal budget process, are compared for the first time. $Si_{1-x}Ge_x$ virtual substrates, having $0.1 < x < 0.3$, are used to compare off-state and on-state device performance. Transconductances and current drive up to 240% higher than control Si MOSFETs are demonstrated. Electron mobility is found to peak using a virtual substrate composition of $Si_{0.75}Ge_{0.25}$.

1. Introduction

Growth of strained Si on SiGe virtual substrates is known to improve carrier mobility and so increase MOSFET current and transconductance. Theoretical studies have suggested that the optimum performance of strained Si/SiGe MOSFETs is achieved by the use of a strained Si surface electron channel and a buried hole channel of compressively strained SiGe [1]. As virtual substrate Ge composition increases, strain relaxation during high temperature MOSFET processing may degrade overall device performance and it is unclear what impact Ge diffusion will have on device operation, particularly if a compressively strained SiGe channel of high Ge composition is used.

2. Device Design and Fabrication

Strained Si n-channel MOSFETs were fabricated on relaxed $Si_{1-x}Ge_x$ virtual substrates (VS) with x = 0.10, 0.15, 0.20, 0.25 and 0.30. The rms surface roughness of the 20% VS was measured as 5 nm using AFM (Fig. 1) and CMP was not used to smooth the cross-hatching. SiGe alloy compositions on fully processed devices were confirmed by SIMS and electron dispersive spectroscopy. Dual channel architectures, comprising a compressively strained $Si_{0.7}Ge_{0.3}$ layer grown between the strained Si surface channel and a $Si_{0.85}Ge_{0.15}$VS were also grown.

Strained Si/SiGe device fabrication followed a conventional 0.25 µm CMOS process. A gate oxide was thermally grown at 800 °C, resulting in a 6 nm gate oxide. Polysilicon was deposited and devices down to 150 nm gate length were patterned using electron-beam lithography. As and P were implanted into the source, drain and gate and annealed at 1050 °C for 20 sec. Back-end processing comprised deposited silox and BPSG with Al metalisation. Control Si devices had a B retrograde well implanted while strained Si/SiGe devices had in-situ doped B ~$7x10^{17}$ cm^{-3}.

3. Electrical Characteristics

Transconductance (g_m) curves as a function of VS alloy composition are shown in Fig. 2a for 0.3 µm MOSFETs. The peak enhancement in maximum g_m (g_m^{max}) over Si control devices is 240% for a $Si_{0.7}Ge_{0.3}$VS at a drain voltage (V_d) = 0.1 V. At V_d = 1.2 V the maximum enhancement in g_m^{max} compared with Si devices is 65% (Fig. 2b). For 10 µm gate length devices the maximum enhancement in g_m^{max} over the Si controls is 120%. The smaller enhancements in g_m^{max} in shorter channel length devices is due to SiGe self-heating. This is illustrated in Fig. 3 by the decrease in drain current (I_d) at higher V_d for the strained $Si_{0.75}Ge_{0.25}$ device, which is not observed for the Si control device. I_d is significantly increased for the strained Si/SiGe device compared with the Si control. At V_g-V_t = 2 V and V_d = 1 V, I_d is 0.65 mA/µm for the $Si_{0.75}Ge_{0.25}$ device and 0.4 mA/µm for the Si control, an enhancement exceeding 60%. The higher channel mobility also causes the lower knee voltage on the I-V curves on Fig. 3.

The field-effect mobility (μ_e) characteristics are shown in Fig. 4. The peak mobility for the strained $Si_{0.75}Ge_{0.25}$ device is enhanced by 115% compared with the peak mobility of the Si control device. These are the first results demonstrating that strained Si MOSFET mobility degrades at higher VS Ge compositions.

The strained Si/SiGe devices exhibited lower threshold voltages than unstrained control devices (Fig. 5). The channel doping in all the devices was designed to be the same and CV measurements (Fig. 6) confirmed that there were no appreciable differences in the electrical oxide thickness (~ 6.5 nm) between the devices shown. The physical oxide thickness is measured as approximately 6 nm by TEM for the $Si_{0.85}Ge_{0.15}$VS MOSFET, in good agreement with the CV data. Therefore the differences in V_t observed are primarily due to the differing electron affinities of the materials, and V_g-V_t was used in comparisons of electrical data.

Fig. 7 shows log I_d vs. V_g–V_t characteristics. The on-state performance is not degraded until the VS Ge composition reaches 30% (Fig. 2) but the off-state performance deteriorates at 20%. Since the sub-threshold characteristic is highly sensitive to the gate oxide interface trap density, the results indicate the effect of Ge diffusion to the surface of the strained Si channel is a negligible until a $Si_{0.7}Ge_{0.3}$ VS is used.

The μ_{fe} - E_{eff} relation for single and dual channel

n-MOSFETs is presented in Fig. 8. The single channel device achieves a higher mobility than the dual channel device over the whole E_{eff} range investigated. At low E_{eff} there is a difference of approximately 10% in the mobility enhancement between the single and dual channel devices. At E_{eff} = 0.8 MV/cm, the enhancement is approximately 50% higher for the single channel compared with the dual channel.

4. Conclusions

On-state performance enhancements of 2-3x in strained Si n-channel MOSFETs compared with Si control devices have been demonstrated for high Ge content virtual substrates (up to 30%). Better electrical performance was exhibited for surface channel devices compared with simultaneously fabricated dual channel devices due to Ge diffusion. Off-state characteristics were shown to be more sensitive to strain relaxation than on-state characteristics.

Acknowledgements

This work is supported by EPSRC.

References

[1] S. Badcock et al., Sol. St. Elec. 46 1925 (2002)

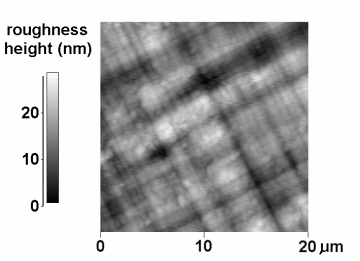

Fig. 1 AFM image of a $Si_{0.8}Ge_{0.2}$ VS

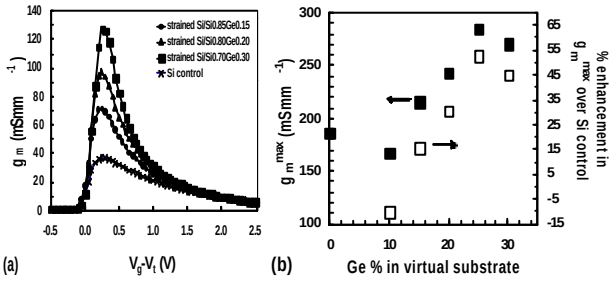

Fig. 2 g_m for 0.3 µm gate length devices: (a) V_d = 0.1 V; (b) V_d = 1.2 V.

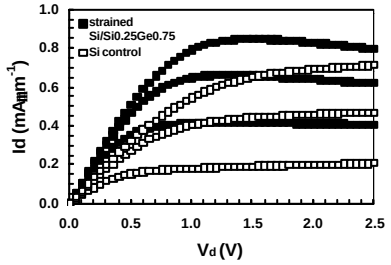

Fig. 3 I_d vs. V_d characteristics for 0.3 µm gate length strained $Si/Si_{0.75}Ge_{0.25}$ and Si control devices measured at V_g-V_t of 1 V, 2 V and 3 V.

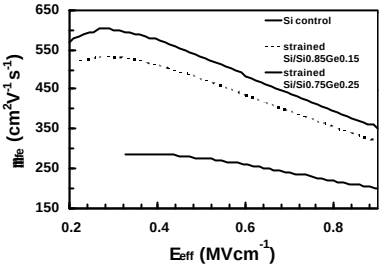

Fig. 4 Mobility-field characteristics of 10 µm gate length devices.

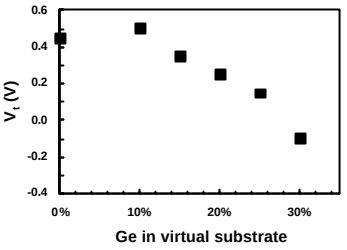

Fig. 5 V_t vs. Ge mole fraction (x) in the $Si_{1-x}Ge_x$ VS.

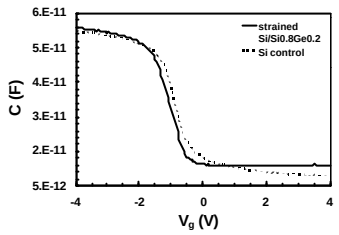

Fig. 6 C-V for 100 µm x 100 µm MOS capacitors

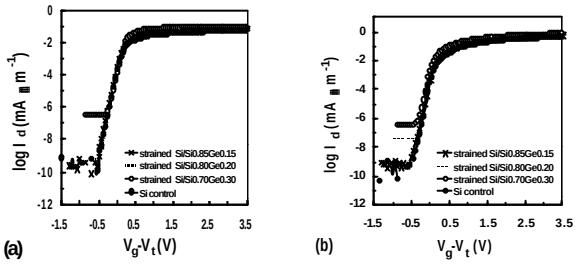

Fig. 7 Log I_d vs. V_g - V_t characteristics for 0.3 µm gate length n-MOSFETs (a) V_d = 0.1 V; (b) V_d = 1.2 V.

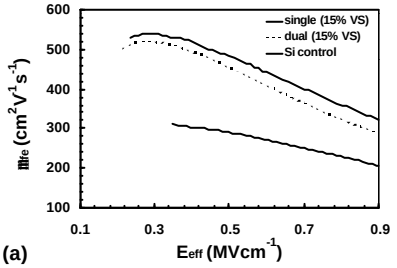

Fig. 8 Comparison of μ_{fe} in single, dual and Si control devices