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Current FeRAM Technology Developments and Scaling towards 3-D Capacitor Cells

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1. Introduction

Ferroelectric memories (FeRAM) have been researched for over 15 years as serious candidates for non-volatile random-access memories, as they offer interesting properties as low-voltage, low-power operation, fast write, and good write endurance. By that, they could offer performance advantages over other non-volatile memories as EEPROM and Flash, while they would be easier to integrate within scaled CMOS technologies.

The development of the process technology for making these FeRAMs, however, has encountered many obstacles. As a result, there are only very few FeRAM products on the market, with very low memory densities (up to 256Kbit stand alone and 64Kbit embedded [1]). Even more advanced development activities are based on CMOS technologies that lag a few generations behind that of advanced logic.

Nevertheless, recently a series of very advanced FeRAM developments have been announced, prototyping already substantial memory sizes ranging till 32Mbit and even 64Mbit [2,3,4]. It is believed that successful completion of these developments will greatly expand the introduction of FeRAM in the market.

In this presentation, the different critical issues for making reliably, high density FeRAMs are pinpointed. The expected roadblocks to a further scaling of the planar capacitor concept are indicated. The technology currently in co-development at IMEC addresses these issues and allows for a more gradual scaling transition from 2-D to 3-D capacitor technology. The development of the MOCVD technology, and initial investigations of its application to form 3-D capacitors are discussed.

2. Evolution of FeRAM Technology Development.

In the development of FeRAM, different stages can be discerned.

Low-density, Offset-Type FeRAM Cell

The development of "first generation" FeRAMs (using CMOS technology of 0.5µm design rule or larger) struggled mostly with basic material reliability problems. Main issue was the poor endurance because of strong electrical fatigue. For PZT, use of metal-oxide electrode or PZT film doping was introduced. Or, SBT was introduced as a new low-fatigue material. Because of large area (using 2T2C), signal density was not a real issue neither was process temperature. For integration, main issue was related to Back-End-Of-Line (BEOL) and Forming Gas Anneal (FGA) compatibility. These issues could be largely alleviated through simple backend process available (only few metal layers, flexibility of choice of dielectric, no W via's for FeCAP contacting, etc.)

Stacked FeRAM Cell

Scaling the FeRAM cell (compatible with technologies in the range of < 0.35µm, aiming at FeRAM denisities of >1 Mb) required stacking of the bottom electrode (BE) plate on top of a plug contact, focusing the work on the development of the conductive oxygen barrier – BE stack. Also, increasing demands on BEOL process required improvements in H-seal and other solutions to prevent BEOL-induced degradation. In a first stage, material considerations were less stringent as (i) major FE material issues were solved, (ii) spin-on or PVD film deposition technology were still adequate, and (iii) memory operation was not yet signal limited (some loss of theoretical maximum Pr could be compensated with larger capacitor area without important penalty on cell area).

Ultimate Scaled 2-D Capacitor Cell

The next generation, that is currently in development, is pushing the limits of 2-dimensional FeCAP's to develop FeRAM densities of >16Mbit. The most critical issue is that memory operation is becoming signal limited, while FeCAP area is already occupying a large fraction of the cell area. Published data furthermore indicates an important drop of signal density with scaled dimensions [4]. While improving the integration technology, as preventing edge damage especially in the 1-mask capacitor etch scheme typically applied, is one factor critical towards signal optimization, a major focus is put again on material optimization as well, as maximal obtainable signal density is required. For technologies below 0.2µm dimensions, material development is further triggered by the need for MOCVD technology for deposition of high-quality thin films (<100nm), even for planar 2-D capacitors.

3-D FeRAM Technology Development

As for the future, we have to develop the 3-dimensional FeRAM. There we will encounter again both technological and FE material issues: technological as for the BE/barrier structure, and material-wise for the application of MOCVD to make high-quality capacitor sidewall material.

3. Ferroelectric Material Selection

As the scaled 2-D capacitor-based FeRAM is becoming signal limited, the choice of the ferroelectric material is an important issue. The two main ferroelectric thin film materials studied are $Pb(Zr_x,Ti_{1-x})O_3$ (PZT) and $Sr_{1-x}Bi_{2+x}Ta_2O_9$ (SBT). These two materials show different advantages and disadvantages as specified in Table I.

The highest available signal density can obviously be obtained by PZT. However, this advantage may be to a large extend lost due to reliability considerations : (i) to obtain low-fatigue, PZT is deposit on metal-oxide electrodes (as IrO_x) resulting in degraded material quality compared to PZT/Pt. Loss of preferential (111) texture indeed reduces 2.Pr to values as low as 20-30µC/cm2; (ii), PZT suffers from a larger charge loss during lifetime (due to imprint). Therefore, SBT is still considered because of superior reliability performance.

Table I Ferroelectric Material Comparison

Material	2.Pr [µC/cm^2]	Process T [^{o}C]	2.Ec [kV/cm]	Imprint rate [6]
PZT	40-60	550-650	150-200	~3
SBT	15-20	700-800	100-150	1
BLT	20-25	600-700	100-150	~1

The main decision factor, however, will be the process temperature. While a good solution for the conductive oxygen barrier are found even withstanding the extended high temperature oxygen anneal required for SBT crystallization [7], compatibility with scaled CMOS for technologies of 0.13µm and below requires lower thermal budget. One solution can be the use of $Bi_{1-x}La_xTiO_3$ (BLT), as maximum temperature may be reduced by more than 50^{o}C, while maintaining excellent reliability (both fatigue and imprint) at even somewhat higher signal [6]. On the other hand, high temperature required for SBT crystallization can be attributed to the 2-step formation process (amorphous deposition followed by crystallization anneal), as 1-step in-situ crystalline SBT-MOCVD deposition has been demonstrated at temperatures as low as 600^{o}C [8].

4. Technology Development at IMEC

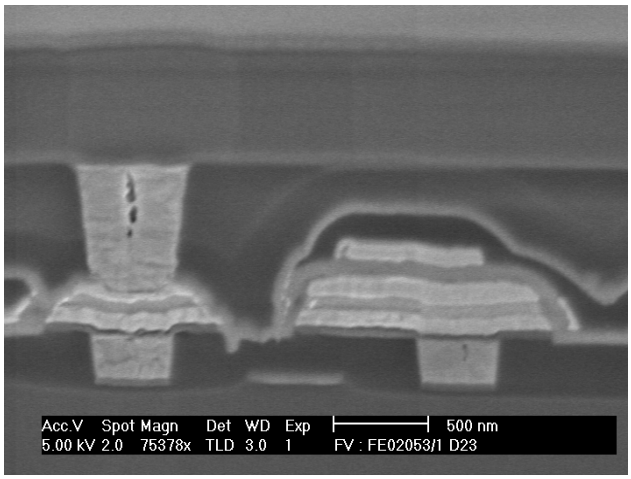

Fig. 1 FIB cross-section of fabricated SBT FeRAM cell

The FeRAM development work at IMEC focuses on a cell concept where the BE is etched prior to the FE film deposition (Fig.1) [5]. Different from the 1-mask capacitor etch, the advantages of our process are (i) use of top electrode (TE) Pt line as common plate line, so that direct contacts to TE are not longer required while number of contact per cell also is strongly reduced, and (ii) scalability to full 3-D cell structure (by increasing BE aspect ratio). The FE material selected is SBT, deposited by MOCVD. The excellent step coverage over pre-etched BE is observed. While comparison of electrical results on test structures with different perimeter/area ratio indicate a contribution of the sidewall material even for our quasi-planar capacitor, sidewall material is not optimized as crystallization of SBT on oxygen barrier material is incomplete (Fig.2) and structural optimization is required [9].

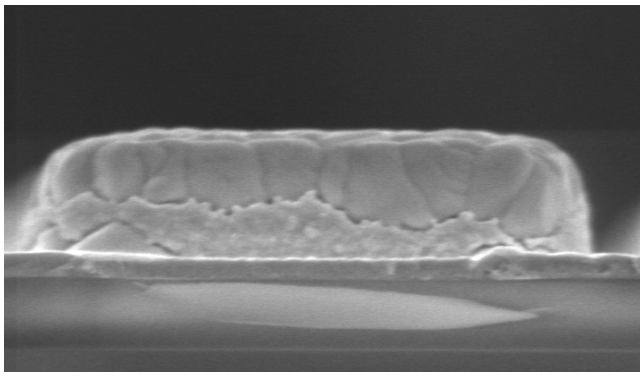

Fig.2 SEM micrograph of crystallized SBT on sidewall

Acknowledgments

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References

[1] See e.g.: www.ramtron.com, www.fujitsu.com

[2] H.McAdams et al., *paper 13-4, 2003 VLSI Circuits Symposium, June 13 2003, Kyoto, Japan.*

[3] Y.Song et al., *paper 12B-1, 2003 VLSI Technology Symposium, June 12 2003, Kyoto, Japan.*

[4] K.Oikawa et al., *paper 13-1, 2003 VLSI Circuits Symposium, June 13 2003, Kyoto, Japan.*

[5] R.Zambrano, *Paper 1.1.1.-I, presented at 15th ISIF, March 9-12 2003, Colorado Springs, USA. To be published in Integrated Ferroelectrics.*

[6] S-S.Lee et al, paper 11.1.1.-I,, *presented at 15th ISIF, March 9-12 2003, Colorado Springs, USA.*

[7] J.Lisoni et al., *paper* 31A-TF7-3C, *presented at the International Joint Conference on the Applications of Ferroelectrics (IFFF 2002), May 28-June 1, 2002, Nara (Japan).*

[8] M.Mitsuya et al, Jpn.J.Appl.Phys. Vol39(2000) pp.L822-824; Nukuga et al, Jpn.J.Appl.Phys. Vol39(2000) pp.5496-5500

[9] J.Lisoni et al., *paper 1.1.2.-C, presented at 15th ISIF, March 9-12 2003, Colorado Springs, USA. To be published in Integrated Ferroelectrics.*