Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 30-31

B-1-2 (Invited)

32Mb Chain FeRAM – An Overview

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1. Introduction

Recently the FeRAM development has shifted more and more to the high density scale, the FeRAM Development Alliance between Toshiba and Infineon has developed a 8M [1] and a 32M product chip [2]. The current focus is on small cell size and high array efficiency to offer a memory technology suitable for high-density stand-alone applications as well as customized system-on-chip solutions. The very low write power consumption of FeRAM is a key feature in portable battery powered and especially so in contactless applications. The applied Chain FeRAM™ architecture is a promising candidate to fulfill all these requirements.

2. Architecture

This paper describes a 32Mb Chain FeRAM fabricated in a 0.2µm 3-metal CMOS process. A small COP ferro cell (capacitor on plug) combined with advanced design features like a compact chain cell block layout and a segment/stitch array architecture allows the realization of a 32M chip with a die size of 96mm^2. Figure 1 shows the cross section of the realized compact chain cell block with significant reduction of the required plate line area by making use of the 3-metal layer process. A wide plate line (PL) as well as the block select line (BS) are realized in M3 together with the stitched word lines (WL0-WL7). The optimized arrangement of the block select transistors gives a further area reduction of the chain block and reduces the bit line capacitance by about 9%. The overall chip area saving adds up to about 4.4%.

The area efficient segment/stitch architecture is shown in Fig. 2. In this 512K array block the M3 layer is used for 1) the main block selector (MBS) signal which realizes the segment array architecture, 2) the stitches for the local word lines and the local block selectors, and 3) the local plate line with low resistance. This array architecture quadruples mat size from 128K to 512K without access time penalty and reduces the overall chip size to 70% compared to the previous chain architecture based on 2 metal layers.

3. Operation

One of the key design issues in FeRAMs is reliable data protection under all operating conditions, especially during power-on/off. A suitable power-on sequence and a reverse power-off sequence were implemented to prevent data loss during ramp up/down of the internal voltages. The boosted word line voltage (VPP) and the word lines are activated first to make sure all the cell transistors are turned on and the ferroelectric capacitors are shorted. Once the cell transistor is in the conducting state the cell capacitor is effectively protected against noise. Subsequently the array voltage (VAA) for BL and PL is activated. Even if noise occurs on BL or PL during power-up of VAA, the cells are effectively shielded and disturb or data loss is prevented.

A sub-0.1µA ultra-low-standby current DC bias generator was implemented in order to minimize the stand-by current consumption which is crucial in mobile applications. A large resistance is used in the feedback loop during stand-by and is switched to a lower resistance when the chip goes into active mode. A sophisticated design of the switchable feedback resistor suppresses switching noise and assures stable operation of this ultra-low-power voltage generator.

Both /CE and address transition triggered access modes are available on the 32M chip providing nearly complete compatibility to a SRAM user interface. The presented chip includes an address transition detector (ATD), which monitors the change of any address pin and activates the chip accordingly. During power-up the implemented interface circuit generates an additional ADT pulse making sure that the data on the outputs corresponds to the applied address even if /CE is continuously activated and no address transition has occurred (Fig. 4). This makes the FeRAM interface yet more compatible to a SRAM. However, write back of the data after read has to be assured in FeRAMs which prohibits full compatibility to static RAMs.

A flexible column redundancy scheme was implemented that can be activated by both laser fuses and electrical fuses based on ferro cells. The redundant columns are located on one edge of the array and can be used over the full column address range. This scheme facilitates a post-package repair of a high number of single bit fails with a limited number of redundant columns and a small area overhead.

4. Results

Figure 5 shows a micrograph of the 32M chain FeRAM chip and some functional blocks like array mat, decoders, drivers and column redundancy areas. The measured random access time is < 50ns at VDD = 3V at room temperature as shown in the Shmoo plot in Fig. 6. Table I. gives an overview of the 32M product specification.

Acknowledgements:

The authors would like to thank all project members of the Infineon/Toshiba FeRAM development alliance for their fruitful support and valuable contribution to this work.

References:

[1] D. Takashima, et al., "A 76-mm2 8-Mb Chain Ferroelectric Memory," IEEE J. Solid State Circuits, Vol. 36, No. 11, pp. 1713 - 1720, Nov. 2001

[2] S. Shiratake et. al., “A 32M Chain FeRAM with Segment / Stitch Array Architecture”, 2003 IEEE International Solid-State Circuits Conference Technical Digest

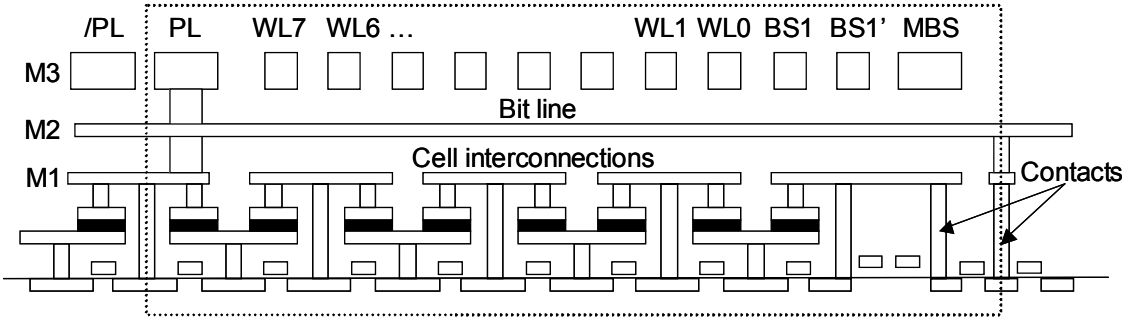

Fig. 1: Cross section of the compact chain cell block layout consisting of 8 cells and a block select transistor.

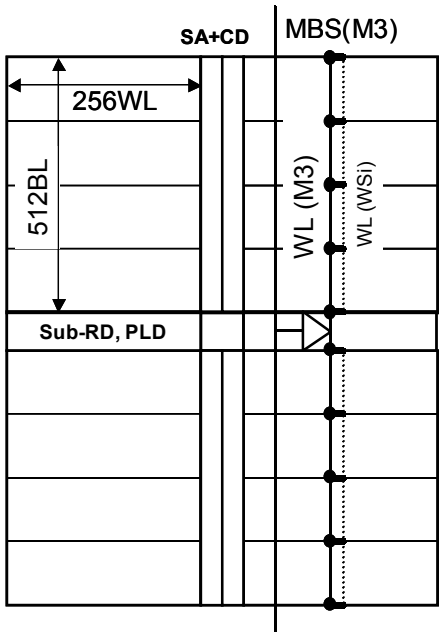

Fig. 2: Area efficient architecture of an array block.

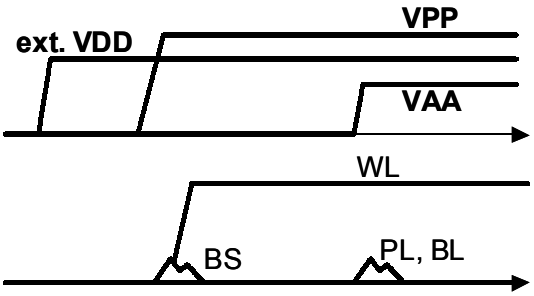

Fig. 3: Power-up sequence for secure operation.

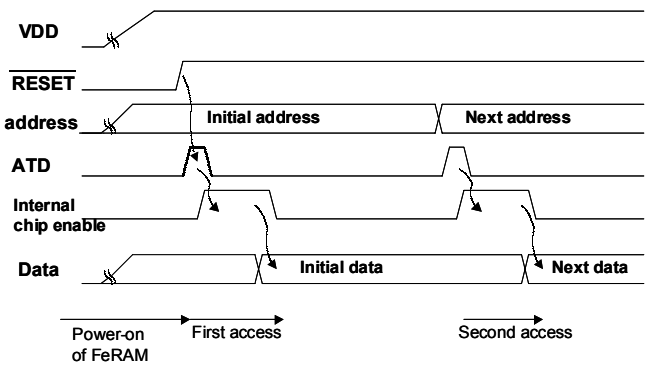

Fig. 4: SRAM compatible interface with ATD (address transition detection) triggered access scheme.

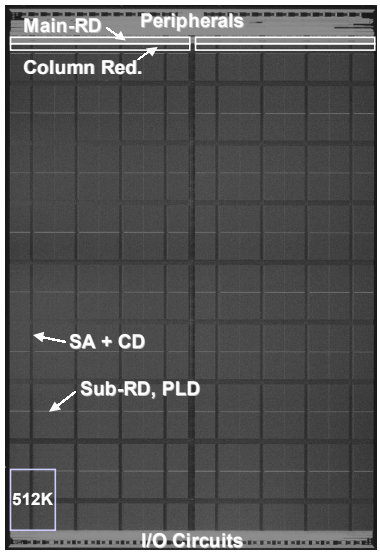

Fig. 5: Die micrograph of the 32M FeRAM chip with a die size of 96mm^2, a cell size of 1.875µm^2 and an array efficiency of 65.6%.

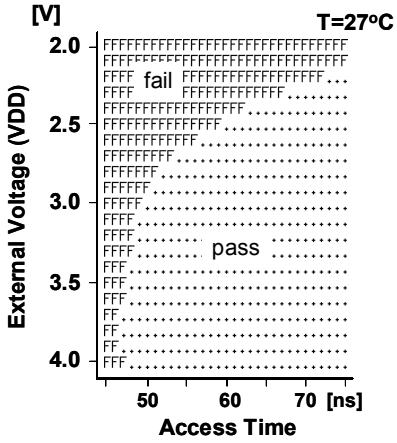

Fig. 6: Shmoo plot of access time vs. external supply voltage.

Tab. I: Product specification data of the 32M chip.

Technology	0.2µm; 1WSi; 3Al
Chip size	96mm2
Cell type	PZT COP
Cell size	1.875µm2 (1T1C)
Organization	2M x 16bit
VDD	2.5/3.0V
tACC	50ns
tCYC	75ns
IDDO	30mA
IDDS	3µA