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A proposal of new ferroelectric gate field effect transistor memory based on ferroelectric-insulator interface conduction

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1. Introduction

One transistor (1T) type FeRAM (ferroelectric gate FET) device has gathered much attention, since this type of memory can advance the integration level of the RAM, keeping the scalability, than the conventional one transistor one capacitor (1T1C) type FeRAM and shows non-destructive read out. However, the metal-ferroelectric (-insulator)- semiconductor (MF(I)S)-FET [1] still has short memory retention time at present stage. The origins for the short retention have been long discussed [2] but the important factor is the effect of interface properties among the M-F-I-S junctions on Si surface channel.

To solve the situation, one idea is to explore a new principle of ferroelectric transistor with nonvolatile memory operation, which does not suffer from damage due to mutual diffusion into Si channel region, and/or has the other operation mechanism more directly related with the ferroelectric polarization reversal then not sensitive to leakage and depolarization field, and so on.

In this paper, a new type of ferroelectric gate FET using ferroelectric-insulator interface conduction has been proposed and is expected to overcome the problems of the MFIS-FET.

2. Proposal of New Ferroelectric FET

The structure of the proposed device is shown in Figure 1. It is basically a Metal-Ferroelectric-Insulator structure on semiconductor (Si) or various materials. This new type of field-effect transistor does not use semiconductor channel but that at interface region between ferroelectric and amorphous insulator [3]. The physical principle behind this device configuration is based on the assumption that the charge compensating the ferroelectric polarization will give two distinct current components for each direction of the polarization. And the polarization charge itself directly give drastic effect on free carriers generated at ferroelectric interface. The insulator can be prepared even on metal, glass or organic materials, as well as semiconductor. Therefore the proposed device can be equipped on various structures, even on curved surface. Also, it simplifies the architecture of the non-volatile ferroelectric memory element by the simple structure.

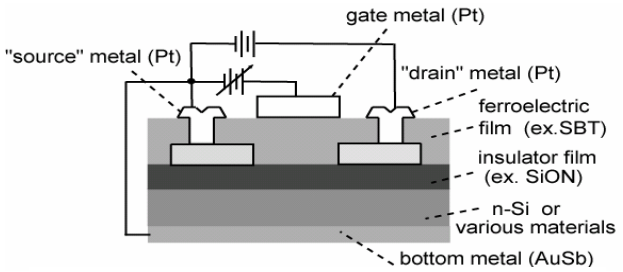

Figure 1. Cross-sectional view of the proposed new ferroelectric

3. Experimental

Silicon oxynitride (SiON) buffer layer was prepared by oxidation at 1000°C for 10s in O_2 ambient and then nitridation at 1000°C for 30 minutes in N_2O ambient. The thickness of SiON film is about 35 nm. Source and drain electrodes of Pt were formed on the SiON by sputtering. Then SBT thin films were deposited on both SiON and the electrodes at 550°C in O_2 atmosphere by pulsed laser deposition (PLD) using a stoichiometric SBT ceramic target. After the PLD deposition, samples were annealed at 600°C in O_2 atmosphere for 30 min. Top Pt electrode and bottom AuSb electrodes are finally formed, respectively. Contact holes to the electrodes were formed by dry and wet etching. Electrical properties of the FET were measured with the Semiconductor Parameter Analyzer (4155C, Agilent).

4. Results and Discussion

Before measurement of drain-to-source current (I_{ds}) behavior in the FET, leakage current through the SBT layer between the gate and drain/source electrodes and the current through the SiON layer between the drain/source and bottom electrodes were checked. As a result, the former was less than 10^{-8}A for the structure of 500μm gate width as shown in Fig. 2, and the latter was in the order of 10^{-9} and 10^{-8}A for 0.02 V and 0.2 V, respectively. Therefore, the leakage through SBT film affects little on I_{ds} when the current I_d is larger than 10^{-8} and 10^{-7}A for drain-to-source voltage (V_{ds}) of 0.02 and 0.2 V, respectively.

Figure 3 shows I_{ds} vs. gate-to-source voltage (V_{gs}) characteristics as a parameter of V_{ds} and figure 4 shows I_{ds} vs. V_{ds} characteristics. It is found from the figures that I_{ds} shows a clockwise ferroelectric (dielectric) hysteresis loop, indicating the ferroelectric polarization in the SBT layer gives drastic effect on I_{ds} value. The ratios of the on-current to the off-current are about 1 order of magnitude for both the curves of V_{ds}=0.2V and 0.02V at sweep rate of V_{gs} of 1.1 V/s. The off-current agrees precisely with the leakage through SiON for both the cases, and so the off current is dominated by the leakage. The current ratios of ON state to OFF state induced by ferroelectric polarization are about 10

and 7 for V_{ds} of 0.02V and 0.2V, respectively, at their transition regions.

The situation of carrier conduction between source and drain is considered to be quite different from the cases of the conventional field effect transistor, in which the carriers exist in crystalline semiconductor. The current behavior in the FET can be explained as follows: 1) Holes flows mainly into the interface between the SBT and SiON because holes would be localized at the interface, considered from the shape of band profile of this stacked Ferroelectric-Insulator structure. 2) When the gate bias is negative, the SBT film becomes polarized, and then free holes are induced in the SBT near the interface as illustrated in figure 5(a) because SBT is typically p-type semiconductor [4]. 3) When the gate bias is positive, on the other hand, the free holes escape away from the channel region as illustrated in figure 5(b) and I_{ds} decreases, because the SBT near the interface is hole-vacant.

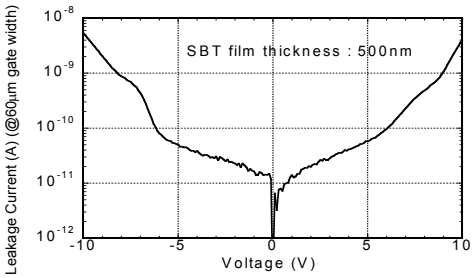

Figure 2. Leakage current from gate to source electrodes through SBT ferroelectric layer.

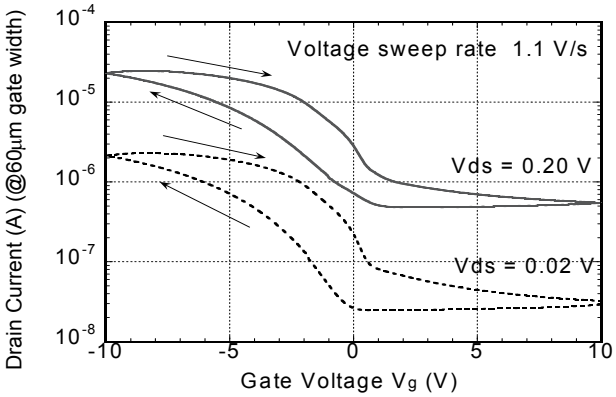

Figure 3. Drain current versus gate voltage of the new proposed FET memory.

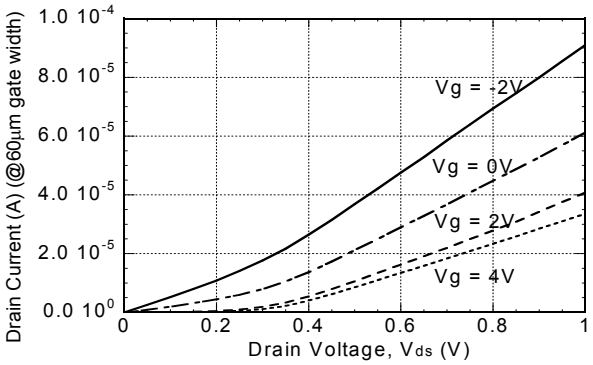

Figure 4. Dain current versus drain voltage.

Threshold voltage (V_{th}) is considered to be a function of Fermi level of SBT layer. So it is difficult to predict V_{th} value at this stage, although it exists around 0 V as shown in figure4. Moreover V_{th} is little dependent on the V_{ds} in the experimental range. It is expected that the ratio of the on-current to the off-current can be more increased by increasing drain-to-source voltage (V_{ds}), although at this stage V_{ds} is limited because of relatively thin SiON thickness of 35 nm. Anyway, further investigation is more needed to understand and improve the conductor phenomena in the FET.

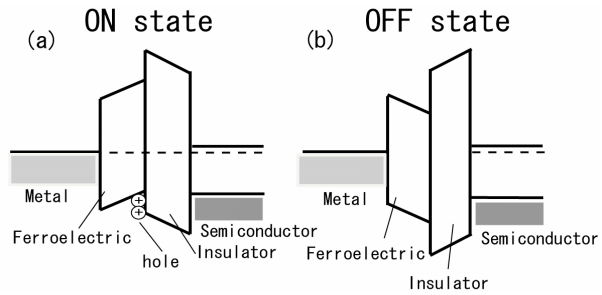

Figure 5. ON and OFF states of band profile of Ferroelectric-Insulator structure.

5. Conclusions

We have proposed and made a new type of ferroelectric gate FET using conduction of ferroelectric-insulator interface region working as its channel. It is found that drain-to-source current is controlled by gate voltage, and that the current is also controlled by ferroelectric polarization effectively. It is expected that this new scheme of FET memory is to be applied for next-generation ULSI's for ubiquitous network component.

Acknowledgements

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