Long-Term Stabilization of Sense Signals in a Non-Destructive Readout FeRAM by Intentional Modification of the Polarization Hysteresis Curve for Low Voltage Applications

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1. Introduction
A non-destructive readout (NDRO) ferroelectric random access memory (FeRAM), in which the read operation is performed by flipping the polarization with a low voltage less than the coercive voltage without polarization reversal, is expected to exhibit an unlimited number of read cycles (> 10\textsuperscript{16}) and a long data retention life (> 10 years) [1,2]. However, the amplitude of the readout signal from a selected cell to be sensed is substantially smaller than that available in conventional destructive readout FeRAMs. Therefore any of electrical degradations in the cell limiting the amplitude of the sense signal would result in an ambiguous logic level. In particular, a gradual deformation of the ferroelectric hysteresis curve with the development of a preferred orientation of polarization, termed imprint, diminishes the amplitude of the differential sense signal [3].

In this paper, we report an asymmetrical programming scheme using asymmetrical remanent polarizations to minimize the imprint effect in an experimentally fabricated 64-kbit NDRO FeRAM.

2. Asymmetrical Programming for NDRO Operation
Ferroelectric capacitors in the 64-kbit NDRO FeRAM are linked in a row to minimize the circuit overhead per cell, as shown in Fig. 1. Two-transistor and two-capacitor (2T2C) cells are configured with complementary pairs of the linked cells. The device parameters are summarized in Table 1. In each 2T2C cell, a pair of a positively saturated value of remanent polarization for a “1” and an intermediate (zero) value of remanent polarization for a “0” is programmed complementary, as shown in Fig. 2. Since the polarization for “0”s has no orientation in polarity, the imprint effect on the polarization for “0”s is no longer expected. Pulse trains for the read operation of a selected cell are illustrated in Fig. 3. To read the data content of the selected cell, a read voltage \(V_{RD}^{\text{min}}\) is determined by the supply voltage \(V_{DD}\) and the upper level of \(V_{RD}\) is limited to 3.5V by an internal drive circuit, is pulsed to a word line (WL) of the linked cells. Within this read voltage range, the voltage \(V_{RD}\) across the selected ferroelectric capacitors is less than the coercive voltage \(V_c\). This mitigates the voltage stress on the ferroelectric capacitors. Following the removal of \(V_{RD}\), the polarization for “1” goes back to its original position. The polarization for “0”, on the other hand, is drawn back to the original position by connecting the floating gate (\(V_c\)) to the gate potential. Thus the NDRO FeRAM does not need any additional rewrite operations after reading.

3. Time Variation in Operation Margin
Using the value of \(V_{RD}^{\text{min}}\) required for reading data without error as a measure of the minimum amplitude of the differential sense signal detectable with the sense circuit among the 64-kbit cells, we examined the time variation in \(V_{RD}^{\text{min}}\) of the NDRO FeRAM programmed with different schemes.

Figure 4 shows three different curves of \(V_{RD}^{\text{min}}\), each corresponding to one of the different programming schemes. When the NDRO FeRAM is programmed using bi-directionally symmetrical polarizations as a conventional manner and subsequently exposed to a temperature of 85°C, \(V_{RD}^{\text{min}}\) increases gradually with time. The increase in \(V_{RD}^{\text{min}}\) after a 1000-h storage is greater than 1.0 V. Then, \(V_{DD}\) is no longer allowed to be less than 2.7V. When the asymmetrical programming scheme described above is used, the increase in \(V_{RD}^{\text{min}}\) is mitigated. The stabilization of \(V_{RD}^{\text{min}}\) with the asymmetrical programming is due to the elimination of the imprint effect on polarizations for “0”s. However, a gradual increase in \(V_{RD}^{\text{min}}\) still remains even if the asymmetrical programming is applied.

4. Intentional Modification of Hysteresis Curve
From the speculation that there is no orientation in the remanent polarization for “0”s when the asymmetrical programming is applied to the NDRO FeRAM, the gradual increase in \(V_{RD}^{\text{min}}\) is attributed to the imprint effect taking place in the polarization for “1”s. To suppress this effect, the polarization hysteresis curves were intentionally modified to prefer “1”s by baking all pairs of capacitors, each preserving a positively saturated value of remanent polarization as a “1”, for an adequate period of time at a sufficiently high temperature. Once the preference of each capacitor to “1” is established, the deformation of the ferroelectric hysteresis curve will not be observed any more. In fact, the NDRO FeRAM undergone the intentional modification of the hysteresis curves exhibited no change in \(V_{RD}^{\text{min}}\) for 1000 h at 85°C, as demonstrated by the lower curve in Fig. 4. This ensures that \(V_{DD}\) can be lowered to less than 2V even if the long-term reliability is considered.

5. Conclusion
The imprint issue in a 64-kbit NDRO FeRAM has been solved completely, when the cells are programmed using an asymmetrical programming scheme and the polarization hysteresis curves are intentionally modified to prefer “1”s prior to high temperature storage tests. As a result, a wide operation range of the supply voltage from 1.8V to 5.5V is available for the NDRO FeRAM by procuring a long-term stability in the amplitude of the differential sense signals.

We like to thank Symetrix Corporation for valuable discussions on the circuit simulation results.

References
Fig. 1 Circuit configuration of a non-destructive readout FeRAM with 2T2C linked cells.

Fig. 2 A portion of a P-V hysteresis curve overlaid with load-lines of the gate capacitance \( C_G \) of an FET for a graphical explanation of non-destructive readout. The ferroelectric capacitor of a selected cell is charged, on the one hand, to a relatively high positive voltage (+\( V_{\text{SET}} \)) to saturate the polarization, representing a “1”; on the other, to a relatively low negative voltage (-\( V_{\text{RST}} \)) to vanish the polarization, representing a “0”. Consequently, the remanent polarizations are asymmetrical each other with respect to the origin. The floating gate potential \( V_G \) is determined by the ratio of the capacitance of the ferroelectric capacitor \( C_f \) to \( C_G \).

Fig. 3 Pulse sequence for the NDRO operation.

Fig. 4 Minimum supply voltage required for reading any cell of the NDRO FeRAM as a function of storage time at 85°C when the NDRO FeRAM is programmed using a symmetrical (bi-directional) programming scheme, an asymmetrical programming scheme, and an asymmetrical programming scheme combined with intentionally modified polarization hysteresis curves.

Table 1. Specifications of the 64-kbit NDRO FeRAM.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.6 µm CMOS</td>
</tr>
<tr>
<td>Ferroelectric Capacitor material</td>
<td>SrBi(_2)(Ta,Nb)(_2)O(_9)</td>
</tr>
<tr>
<td>area</td>
<td>3.0 x 3.0 µm(^2)</td>
</tr>
<tr>
<td>thickness</td>
<td>200 nm</td>
</tr>
<tr>
<td>Supply Voltage ( V_{\text{DD}} )</td>
<td>1.8 – 5.5 V</td>
</tr>
</tbody>
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