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A Low Dielectric Constant $Sr_2(Ta_{1-x},Nb_x)_2O_7$ Thin Film Controlling the Crystal Orientation on IrO_2 Substrate for One Transistor Type Ferroelectric Memory Device

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1. Introduction

Recently nonvolatile memory devices having ferroelectric gate structure (Metal- Ferroelectric- Metal- Insulator Field Effect Transistor (MFMIS-FET) structure) have attracted much attention from the viewpoints of high speed, nondestructive readout and high-packing-density memory LSIs. However it has been difficult to operate an MFMIS-FET at low voltage because the ferroelectric film has a high dielectric constant [1]. We have selected $Sr_2(Ta_{1-x},Nb_x)_2O_7$ (STN, x=0.3) as a ferroelectric material because it has a low dielectric constant [2],[3] and we have reported the fundamental ferroelectric characteristic of the STN film formed by a modified plasma PVD and oxygen radical treatment [4]. Furthermore, in order to obtain a large memory window using a very thin ferroelectric film, it is necessary to obtain a large coercive field. That is, for realization of one transistor type (1T-type) ferroelectric memory, development of the process technology for acquiring a target characteristic value of ferroelectric (a low dielectric constant and large coercive field) is indispensable.

In this work, we report the new technology that controls the orientation of STN and the property of the STN with a low dielectric constant and large coercive field formed on the IrO_2 substrate. We also report the characteristics of the MFMIS device for realizing an 1T-type ferroelectric memory. The MFMIS device has a large memory window and a long retention time.

2. Experimental

Fig.1 shows a concept of achieving the STN film with a low dielectric constant and large coercive field by controlling the crystal orientation. We have controlled the STN crystal orientation by controlling the substrate crystal orientation. The prepared substrates were $Pt/IrO_2/SiO_2/Si$ substrate (Pt substrate), $Ir/IrO_2/SiO_2/Si$ substrate (Ir substrate), $IrO_2/Ir/IrO_2/SiO_2/Si$ substrate ($IrO_2/Ir/IrO_2$ substrate) and $IrO_2/SiO_2/Si$ substrate (IrO_2 substrate) as sown in Fig.2. The STN(150nm) films were formed on these substrates by the plasma PVD process [4] in which the mixing ratio of $O_2/(Ar+O_2)$ and working pressure were 6% and 4Pa, respectively. The STN films were crystallization-annealed at 950℃ for 90min in the oxygen ambient. Identification of the crystallographic phase and its orientation was performed by an XRD reciprocal space mapping [5]. Moreover, Al/STN (260nm)/IrO_2 (65nm)/SiO_2 (13nm)/Si (n-Type) MFMIS structure devices were fabricated.

3. Results and Discussions

Fig.3 (a) shows XRD reciprocal space mapping of the STN on the Pt substrate. This result shows that the STN ($A_2B_2O_7$ type perovskite slab structure) grows as a main phase and its orientation is (102). However, the other different phase from the STN perovskite phase grows a little. Fig.3 (b) shows the mechanism of the (102) oriented STN crystal growth on the (111) oriented Pt. The STN's a-axis lattice parameter (0.395nm) nearly matches the lattice parameter of Pt (0.392nm).

Fig.3 (c) shows XRD reciprocal space mapping of the STN on the IrO_2 substrate. This result indicates that the (111) and (0$\underline{14}$1) oriented perovskite STN is formed as a main phase and other different phase from STN perovskite phase cannot be observed at all. The measurement result of XRD reciprocal space mapping of the STN on the Pt, Ir, $IrO_2/Ir/IrO_2$ and IrO_2 substrates is summarized in Table1. In the case of the Ir and $IrO_2/Ir/IrO_2$ substrates, it is very difficult for the STN perovskite phase to grow up as main phase in the film. This indicates that the oxygen in the STN reacts with Ir and the oxygen is lacked. On the other hand, in the case of the IrO_2 substrate, we can obtain the STN perovskite phase with a more effective orientation. That is, compared to the Pt substrate, the angle between the c-axis of the STN and the IrO_2 substrate is considerably smaller.

Fig.4 shows C-V characteristic of the STN capacitors on the Pt and IrO_2 substrates. The dielectric constant of the STN on IrO_2 (ε_r=35) is lower than that on Pt (ε_r=44) and these results are due to the orientations of the STN films.

Fig.5 shows D-E hysteresis loops of the STN capacitors on the Pt and IrO_2 substrates at 1kHz [4]. For the IrO_2 substrate, the average remanent polarization (P_r) is 0.6μC/cm^2 and the coercive force (E_c) is 59kV/cm when applied electric field is 400kV/cm. For the Pt substrate, the P_r is 0.4μC/cm^2 and the E_c is 17kV/cm by the same measurement conditions.

Fig.7 shows C-V characteristics of the MFMIS structure device as shown in Fig.6 at 1MHz. A counter clockwise C-V hysteresis is observed and its memory window is 1.3V at a sweep voltage of ±5V. Fig.8 shows the variation of the capacitance value of the MFMIS structure device when the holding gate voltage is +1V after a writing operation with +5V or –5V bias. More than 10 hours retention time can be obtained.

4. Conclusion

We have successfully developed a new technology that controls the crystal orientation of the STN on the IrO_2 electrode and realizes the STN film with a low dielectric constant (ε_r=35) and a large coercive field (E_c=59kV/cm). Furthermore, the MFMIS structure device with a large memory bias window (1.3V) under ±5V operation and a long retention time (>10hours) has successfully been fabricated. This STN film is a most practical candidate for one transistor type ferroelectric memory device.

References

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[5] K. Saito et al, Jpn. J. Appl. Phys., vol. 39, p. 5489 (2000)
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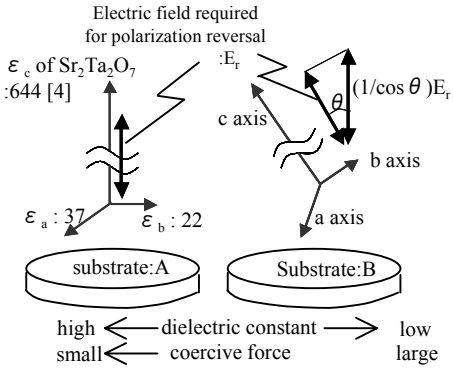

Fig.1 A concept of achieving the STN film with a low dielectric constant and large coercive field by controlling the crystal orientation.

Table.1 (a) Identification of the crystallographic phase and its orientation.

substrate	STN perovskite phase					Other phase	
	Relative Volume [%]	Information of orientation			The expected polarization value **	phase	Relative Volume [%]
		orientation	θ [°]*	Relative Volume[%]			
Pt/IrO2	**81**	(102)	54.4	100	0.66	$Sr_7(Ta,Nb)_6O_{21}$	19
Ir/IrO2	27	(112)	54.1	100	0.22	$Sr_5(Ta,Nb)_4O_{15}$	**73**
IrO2/Ir/IrO2	60	(110)	0	95	0.01	$Sr_5(Ta,Nb)_4O_{15}$	**40**
		(0141)	18.8	5			
IrO2	**100**	(111)	34.6	32	0.28	——	0
		(0141)	18.8	31			
		(100)	0	5			
		(010)	0	15			
		(110)	0	18			

*the angle between c-axis of the STN and the substrate

* * Normalized by the polarization value which is obtained when the (001) oriented STN is grown.

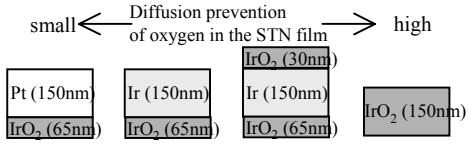

Fig.2 Device structure images of four substrates ($Pt/IrO_2/SiO_2/Si$, $Ir/IrO_2/SiO_2/Si$, $IrO_2/Ir/IrO_2/SiO_2/Si$, $IrO_2/SiO_2/Si$).

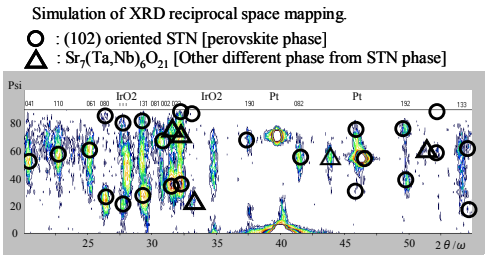

Fig.3 (a) XRD reciprocal space mapping of the STN on the Pt substrate ($Pt/IrO_2/SiO_2/Si$).
The (102) oriented STN perovskite phase grows as a main phase. However, the other different phase from the STN perovskite phase grows a little.

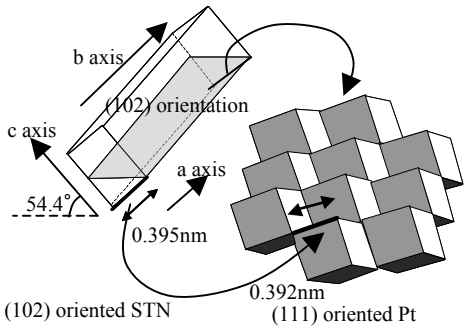

Fig.3 (b) The mechanism of the (102) oriented STN crystal growth on the (111) oriented Pt.
The STN's a-axis lattice parameter nearly matches the lattice parameter of Pt.

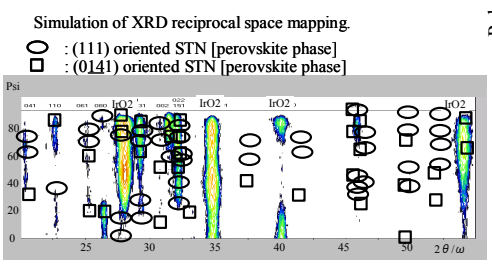

Fig.3 (c) XRD reciprocal space mapping of the STN on the IrO_2 substrate ($IrO_2/SiO_2/Si$).
The (111) and (0141) oriented perovskite STN is formed as a main phase and other defferent phase from STN perovskite phase cannot be observed.

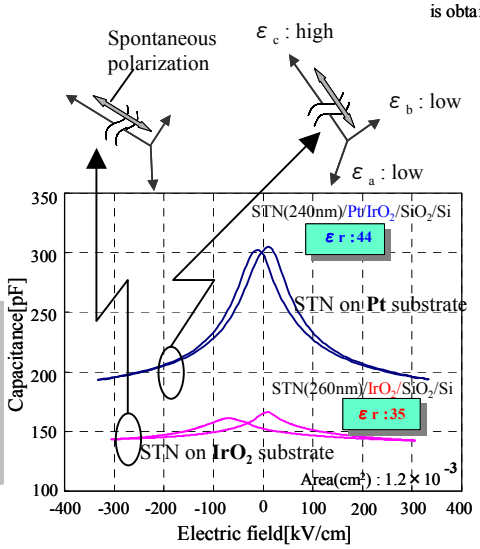

Fig.4 (a) C-V characteristic of the STN capacitors on the Pt and IrO_2 substrates.
The dielectric constant of the STN on IrO_2 (ε_r=35) is lower than that on Pt (ε_r=44) and these results are due to the orientations of the STN films.

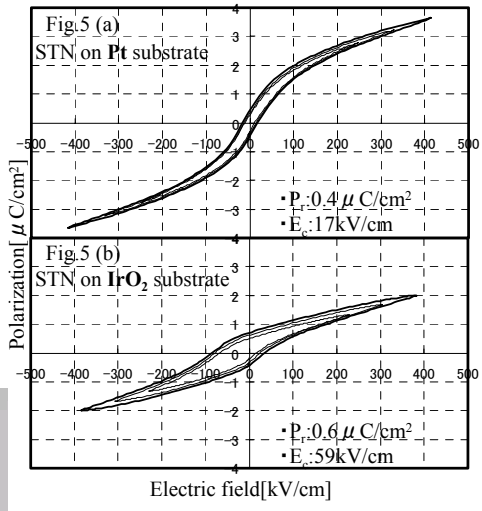

Fig.5 D-E hysteresis loops of the STN capacitors on the Pt(a) and IrO_2(b) substrates.
In the case of the STN on IrO_2, the E_c is 59kV/cm when applied electric field is 400kV/cm.
In the case of the STN on Pt, the E_c is 17kV/cm.

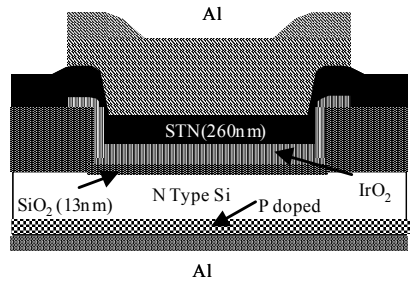

Fig.6 Device structure images of the MFMIS structure.

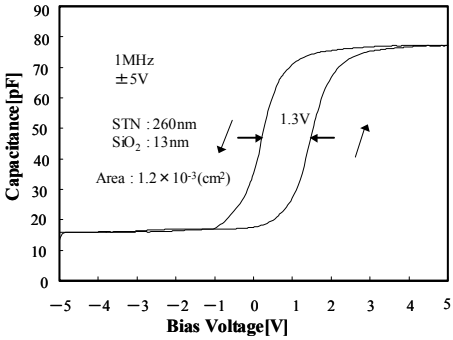

Fig.7 C-V characteristics of the MFMIS structure device . The memory window is 1.3V at a sweep voltage of ±5V.

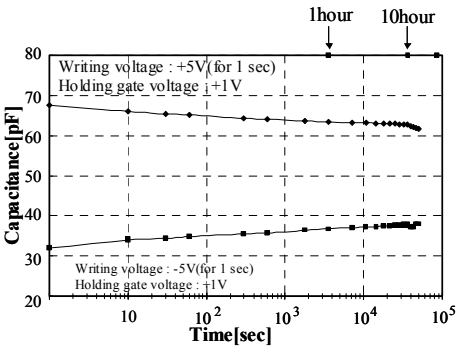

Fig.8 The variation of the capacitance value of the MFMIS structure device when the holding gate voltage is +1V after a writing operation with +5V or –5V bias.
More than 10 hours retention time can be obtained.