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Low-Noise and High-Frequency 0.10μm body-tied SOI-CMOS Technology with High-Resistivity Substrate for Low-Power 10Gbps Network LSI

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1. Introduction

Recently, a system on a chip (SOC) for network LSI, which includes high-frequency analog and digital circuits is taken noticed widely (Fig.1). As for high-frequency I/O operation, power consumption increases with raising the frequency, and increase of power consumption becomes a critical issue because of expensive cooling equipment. Therefore, low-power chip is desired.

In this paper, we indicate the distinct validity of the high-performance and low-power silicon-on-insulator (SOI) device on SOC for network LSI. A 0.10 μm SOI CMOS technology with hybrid trench isolation (HTI) on high-resistivity substrate was developed. Low CoSi2 resistance (5Ω/□) without anomalous junction leakage current was achieved for high radio-frequency (RF) characteristics. High Q-factor varactor was realized by optimization of drain edge structure with eliminating pocket implantation. Moreover, validity of lowering body resistance in body-tied structure is indicated for suppression of the phase noise. By using these technologies, high-frequency (over 10Gbps) and low noise operation such as excellent eye pattern of output buffer circuits on high-resistivity (HR) substrate was obtained for the first time.

2. Experiment

High-resistivity substrate over 1000Ω･cm was used for SOI substrate. Dual oxide process for 1.2V/3.3V SOI MOSFETs was adopted. HTI technology was applied for body-tied structure [1][2]. Pocket/extension implantations for drain structure were used for 1.2V MOSFETs. CoSi2 was used on gate and source/drain (S/D) regions. No-kink in Id-Vd characteristics and high breakdown voltage of S/D were realized even at 3.3V by using body-tied structure [3].

3. Results and Discussion

A. Improvement in fmax of MOSFET and Q-factor of varactor

Key technologies for the network LSI on SOI substrate are summarized in Table Ⅰ. To realize low-noise and low-power circuit, the fmax of MOSFET and the Q-factor of passive elements need to be improved. Fig. 2 and 3 show a current-mode buffer circuit and a LC-tank voltage-controlled-oscillator (VCO) for communication LSI [4]. Current-mode buffer circuits require high fmax of MOSFET. The power consumption of the circuit can be suppressed by current reduction and low supply voltage. Fig. 4 shows measured Lg dependence of fmax on SOI MOSFET. For shortening Lg, fmax was raised because of improvement in gm. Active current can be lowered for shorter Lg to maintain high-frequency operation. As a result, estimated power consumption of current-mode buffer circuit by a product of V and I can be suppressed as shown in Fig.5.

Reducing the gate resistance can improve fmax of SOI MOSFET. Fig. 6 shows the relation between fmax and sheet resistance of CoSi2 on gate electrode. About 33% improvement of fmax was obtained by the resistance reduction from 9Ω/□ to 5Ω/□ owing to the thicker sputter-Co and/or the high-temperature rapid thermal annealing. Based on the technology, 150 GHz fmax was achived with 100nm gate SOI MOSFET. Although these approaches may cause junction leakage current, anomalous leakage current was not observed in our devices because of no junction area under the S/D regions.

High-quality passive elements such as spiral inductors and varactors are also important to realize for high-performance network LSI. Characteristic of varactor dominates the VCO performance. We propose new design guideline of MOS varactor for high Q-factor. Fig. 7 shows a schematic diagram of n-type varactor on SOI substrate. Fig. 8 shows the measured Q-factor and parasitic resistance of n-type varactors with different pocket implantation dose. It is found that the resistance is suppressed and Q-factor is improved by lowering pocket implantation dose. In the depletion bias condition (Vg=-0.5V), ratio of improvement is higher than that of accumulation bias condition (Vg=0.5V). To investigate the effect of pocket implantation dose, device simulation was performed. Fig. 9 (a) shows the simulated current density distribution near the drain edge region with pocket implantation (Vg=-0.5V). It is found that the current flows not only near the gate oxide interface but also in body portion. Fig. 9 (b) shows depth profile of the current density at the drain region (x=0.2μm) for comparison with/without the pocket implantation. This indicates Q-factor of the structure without pocket implantation is higher than that with pocket implantation because of low body resistance.

B. Low noise 10Gbps operation

Phase noise of the circuit is a critical issue for network LSI. The phase noise can be divided into two kinds of constituents such as a deterministic jitter and a random jitter. History effect of the SOI MOSFET would be one of the origins for deterministic jitter. After the body potential modulation by the coupling from gate and drain switching, it must be recovered by the next signal for stable operation. Fig. 10 shows simulated waveforms of the input buffer circuit of five-stage configuration with high and low body-resistance. In the case of the high body-resistance, large deterministic jitter is observed in the output waveform compared to that of the low body-resistance. To analyze the deterministic jitter, the each node potential is indicated in Fig. 11. The body potential at the 1st stage buffer circuit is modulated by the variation of the input signal intervals, and affects the drain potential modulation. The modulation is amplified, and the deterministic jitter of the output signal at the last stage becomes large owing to the high body-resistance. Therefore, lowering body resistance owing to shorten finger length is effective for the realization of the stable circuits operation with low deterministic jitter.

Random phase noise of a SOI circuit can be improved by using high-resistivity substrate that achieves high Q-factor of spiral inductor. In Fig. 12, measured random jitter of output waveform on high-resistivity substrate is compared to that on 10Ω･cm substrate. The jitter was suppressed by about 15%. This result is considered that the Q-factor improvement of the spiral inductor is a main contribution [†] [5]. Fig. 13 shows the measured output signal waveform from the current-mode output buffer circuits. 10Gpbs operation with excellent eye pattern showing low jitter and steep Tr/Tf of 24.0/21.8 psec were realized at Vdd=1.2V. The jitter improvement by lowering body resistance and the high-resistivity substrate has a large influence on the performance of high-frequency network LSI.

4. Conclusion

High-frequency operation (10Gbps) and low phase noise (10psec) SOI device technology was developed. 150GHz fmax was achieved in 100nm gate MOSFET with low resistance CoSi2. Low phase noise was obtained by low body resistance and by high Q-factor of the varactor on high-resistivity substrate. This technology has a great potential for the realization of high performance network LSI.

5. Appendix †$L(\Delta\omega)=10 \cdot \log((2kT/P) \cdot (\omega_0/2Q\Delta\omega)^2)$ $L(\Delta\omega)$: phase noise P : average power dissipation, ω_0 : carrier frequency, $\Delta\omega$: offset frequency, Q : Q-factor Ref.[5]

References [1] S. Maeda, et al. :Symp. VLSI Tech. Dig., p.92 (2000).
[2] Y. Hirano, et al., :IEDM Tech. Dig., p. 467 (2000). [4] T. Yoshimura, et al. : Proc. CICC, p.355 (2002).
[3] S. Maeda, et al. :Ext. Abst. SSDM, p.270 (2001). [5] T. H. Lee : The Design of CMOS Radio-Frequency Integrated Circuits, p534.

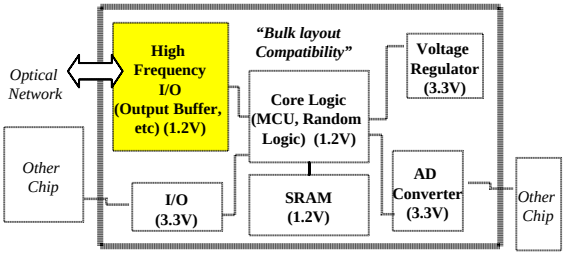


Fig.1 Block Diagram of network LSI on SOI substrate.

Table Ⅰ Key technologies for network LSI on SOI substrate

Technology	Characteristics	Performance
Short gate length SOI Tr.	High ft, fmax (High gm)	Low Power
Low resistivity CoSi2 on gate and S/D without amomulus junction leakage current on SOI	High fmax (Low power loss)	Low Power
No pocket implantation of varactor	High Q-factor (Low resistance)	Low Noise
Low body resistance of hybrid trench isolation	Suppresion History Effect	Low Noise
High resistivity SOI substrate	High Q-factor, High ft, fmax	Low Noise

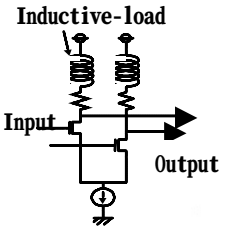


Fig.2 Current mode buffer circuit

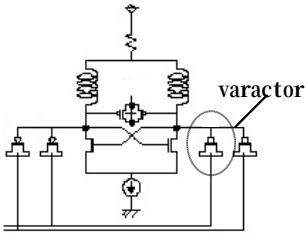


Fig.3 LC-VCO circuit [4]

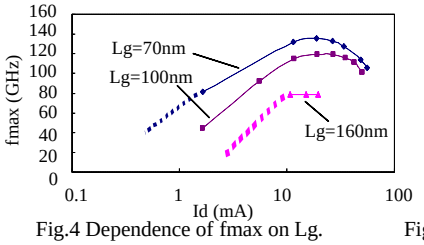


Fig.4 Dependence of fmax on Lg. Current of the short channel MOSFET can be reduced with keeping high fmax charactristics. Sheet resistance of CoSi2 on gate is 9Ω/□.

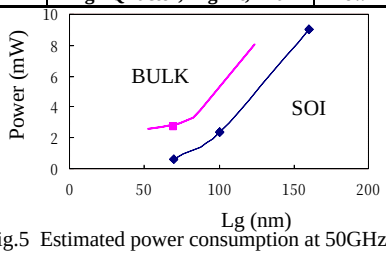


Fig.5 Estimated power consumption at 50GHz fmax of a current mode circuit as shown in Fig. 2. The power consumption of the current mode circuit can be decreased by shortening Lg because active current is lowered.

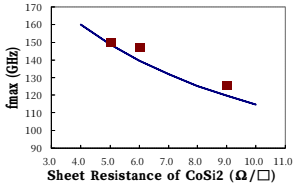


Fig.6 fmax vs. sheet resistance of CoSi2 on gate electrode. fmax is improved by reduction of CoSi2 resistance.

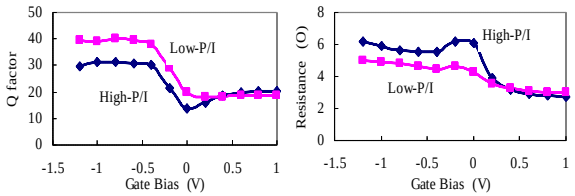


Fig.8 Q-factor and parasitic resistance of the n-type varactor. The parasitic resistance is reduced, and Q-factor is increased with reduction of the pocket implantation dose (P/I).

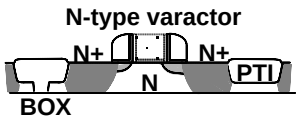


Fig.7 Schematic diagram of SOI n-type varactor.

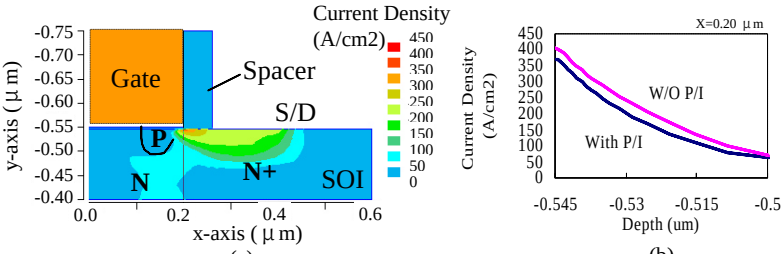
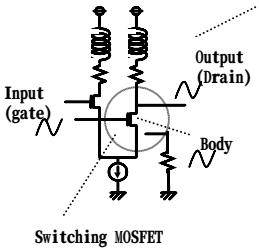


Fig.9 (a)Simulated current density distribution of the n-type varactor which includes pocket implantation (P/I). (b) Depth profile of the simulated current density at the drain edge region (X=0.20 μm) of the n-type varactors with and w/o pocket implantation. (@Vg=-0.5V, Vs=0V)



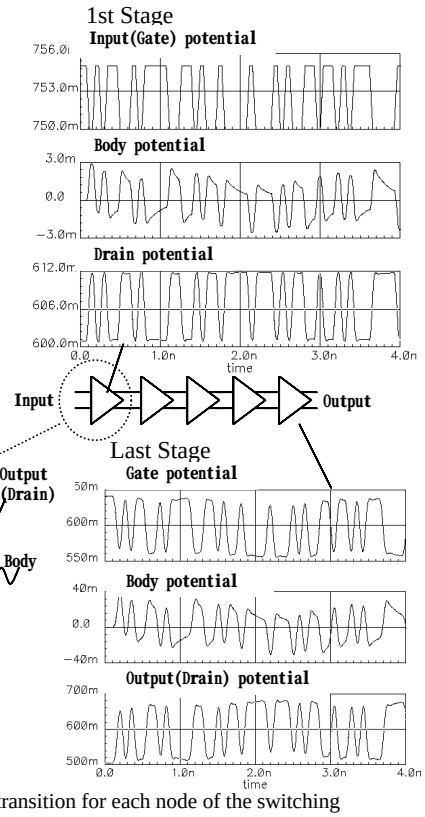


Fig.11 Simulated potential transition for each node of the switching MOSFET in the input buffer circuit with long finger layout (high body resistance). Simulated circuit is the five-stage current-mode buffer circuit.

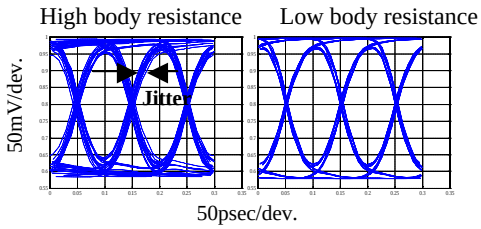


Fig.10 Simulated waveforms of input buffer circuit. Jitter of circuit with lowering body resistance can be improved by using short finger layout.

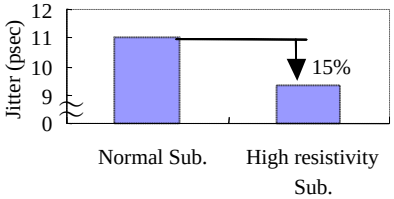


Fig.12 Measured jitter of output waveform from network LSI. Jitter is reduced by high-resistivity substrate.

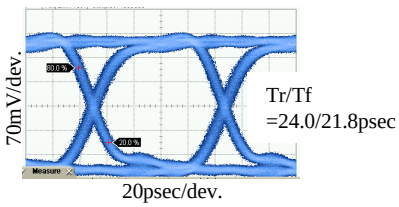


Fig.13 Measured waveform of output buffer circuit. 10Gbps operation is achieved at 1.2V. Lg=100nm.