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Fully Depleted SOI CMOS Device with Raised Source/Drain for 90nm Embedded SRAM Technology

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Abstract

The characteristics of fully depleted (FD) SOI devices with 60nm gate length for 90nm embedded SRAM technology were investigated for different SOI film thicknesses. Selective epitaxial growth (SEG) process was well optimized to maximize the device performance in the process flow points of view. Transistor performance of 640mA/mm and 270mA/mm at 1.0V operation and Ioff=10nA/mm was obtained for NMOS and PMOS devices, respectively. DIBL was improved as scaling down the SOI film thickness to 15nm. The static noise margin, the cell current and the maximum dynamic drain current for a 1.1mm^2 SRAM cell were 190mV, 35mA, and 5 mA, respectively.

Introduction

SOI technology is penetrating the commercial market and has been included in the microelectronics roadmap as the most realistic solution for nano CMOS devices [1]. SOI device are suitable for low power and high performance applications [1-5]. Fully depleted (FD) SOI devices have excellent short channel behavior and diminished floating body effect (FBE) over the partially depleted SOI and bulk Si devices [2]. The raised source/drain process with Si selective epitaxial growth (SEG) is necessary to reduce the parasitic series resistance and improve the performance of the FD-SOI devcies [2]. In this paper, FD-SOI CMOS SRAM technology with the optimized raised source/drain for 90nm technology node is investigated in terms of scaling of SOI film thickness

Fabrication Process

The starting material was SIMOX SOI wafer with 80nm and 135nm in thickness for SOI and BOX layers, respectively. Device fabrication process flow is summarized in Fig.1. The SOI thickness at channel region was ranging from 36nm to 15nm. Thin gate dielectric with the thickness of 1.6nm was formed by thermal oxidation and nitridation annealing. Si SEG process for the raised source/drain was applied to compare the effect of parasitic series resistance before (SEG-A process) or after (SEG-B process) deep source/drain implant. Figure 2 shows the cross sectional SEM image of FD-SOI transistor with 60nm gate length formed on 35nm SOI layer. Cu interconnects and low-k dielectrics were applied to fabricate SRAM chip with the cell size of 1.1mm^2.

Result and Discussion

SEG profiles of SRAM cell arrays for SEG-A and SEG-B processes with 60nm gate length devices on 35nm SOI are shown in Fig 3 (a) and Fig. 3 (b), respectively. Epi-Si profile formed by SEG-A was more satisfied than that formed by SEG-B process. For SEG-B process, Si agglomeration was found at active region. As shown in Fig. 4, the threshold voltage(Vth) shift by SEG-B process was observed, especially in PMOS due to born penetration. This indicates the fact that thermal budget of SEG-B process was larger than that of SEG-A process. Figure 5 and Figure 6 show transistor performance of NMOS and PMOS SOI devices. For SEG-A process, the NMOS and PMOS performance were improved to be 15 and 20%, respectively, compared to the SEG-B process. The extension sheet resistance of SEG-A devices was lower than that of SEG-B devices shown in Fig. 7. Figure 8 shows typical sub-threshold characteristics of NMOS and PMOS FD-SOI transistors with gate length of 60nm and the optimized raised source/drain process. The sub-threshold swing values of NMOS and PMOS were 79 and 78mV/dec., respectively. As shown in Fig. 9 and Fig. 10, for SOI devices with SOI thickness of 35nm, no kink effects were observed in Ids-Vds curve and output conductance characteristics, respectively. Figure 11 shows drain induced barrier lowering (DIBL) characteristics of NMOS with different SOI thicknesses and gate lengths. The DIBL value was decreased from 100mV to 33mV, when SOI thickness varied from 100nm to 15nm. At the same Vth value, the DIBL for SOI devices with thickness of 15nm were drastically decreased over the 35nm SOI thickness devices shown in Fig.12 (NMOS) and Fig.13 (PMOS). The characteristics of 1.1μm^2 SRAM cell show the highly stable butterfly curve with 190mV static noise margin, the 35μA cell current (Icell), and the 5μA maximum dynamic drain current (Idd.max), as showing in Fig. 14.

Conclusion

FD-SOI CMOS device with 60nm gate length and optimized raised source/drain for 90nm embedded SRAM technology were investigated. Si selective epitaxial growth process before deep source/drain implant is greatly recommended for excellent device performance with reduced series resistance. Drain induced barrier lowering is drastically decreased by reducing SOI thickness. Transistor performance of 640μA/μm and 270μA/μm at 1.0V operation and Ioff=10nA/μm was obtained for NMOS and PMOS devices, respectively. The static noise margin, the cell current and the dynamic maximum drain current for the 1.1μm^2 SRAM cell were 190mV, 35μA, and 5 μA, respectively.

References

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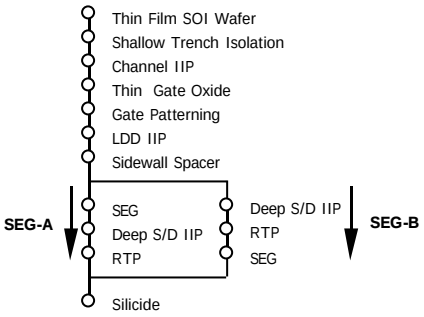

Fig.1 Device fabrication process flow and SEG process step experiment

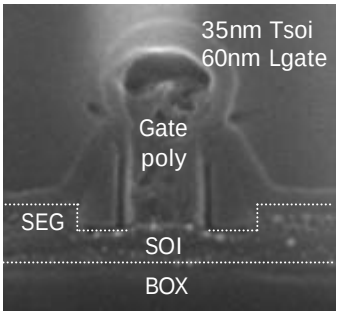

Fig.2 Cross sectional SEM image of FD-SOI transistor

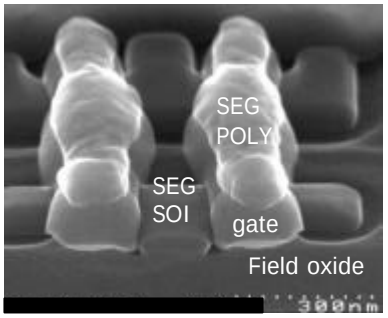

Fig.3 (a) SEG profiles at 1.1 μm^2 SRAM cell array with SEG-A process

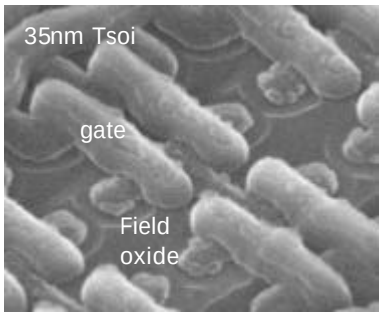

Fig.3 (b) SEG profiles at 1.1 μm^2 SRAM cell array with SEG –B process

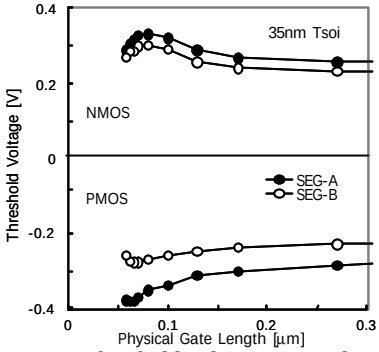

Fig.4 Threshold voltage vs. gate length for SEG-A and SEG-B process

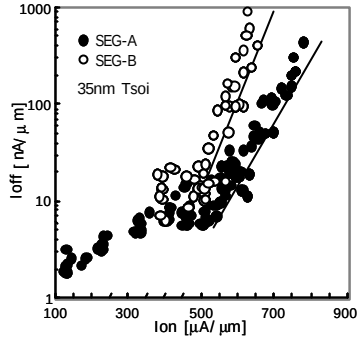

Fig.5 NMOSFET performance as Ioff versus Ion in terms of SEG process

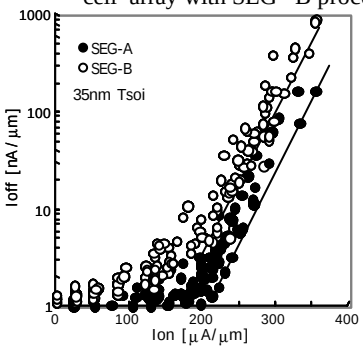

Fig.6 PMOSFET performance as Ioff versus Ion in terms of SEG process

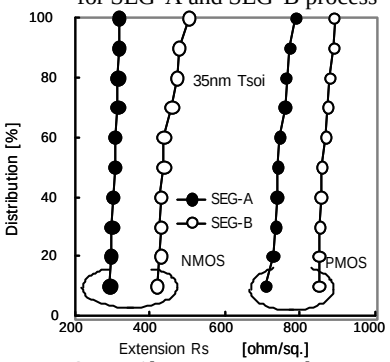

Fig.7 Source/drain extension sheet resistance in terms of SEG process

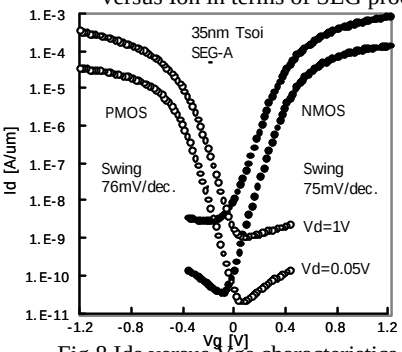

Fig.8 Ids versus Vgs characteristics of NMOS and PMOS

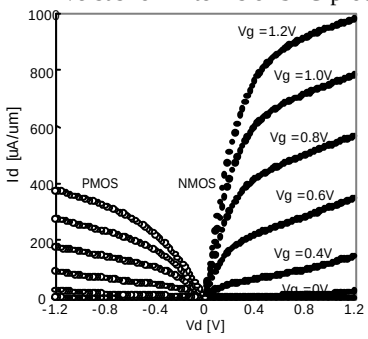

Fig.9 Ids versus Vds characteristics of NMOS and PMOS

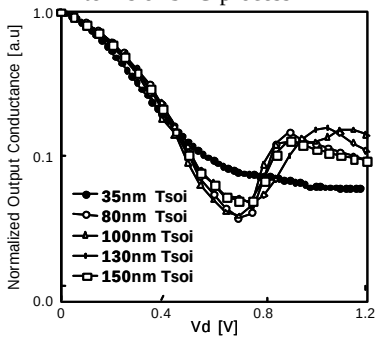

Fig.10 Output conductance characteristic of NMOS with respect to SOI thickness

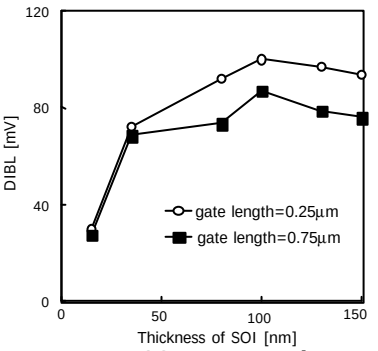

Fig.11 NMOSFETs DIBL characteristics with respect to SOI thickness

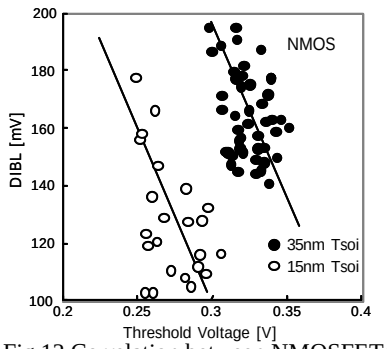

Fig.12 Correlation between NMOSFETs DIBL and Vth value (Lgate = 60nm)

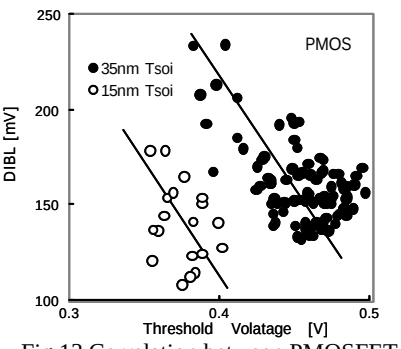

Fig.13 Correlation between PMOSFETs DIBL and Vth value (Lgate = 60nm)

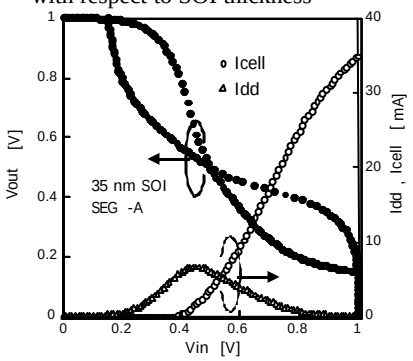

Fig.14 1.1μm^2 SRAM cell characteristics