Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 758-759

B-10-4

Body Contact Structure using Elevated Field Insulator for Ultra-Thin Film SOI-MOSFETs

S. Yamagami, R. Koh, H. Wakabayashi, J.-W. Lee, Y. Saito[1], A. Ogura
M. Narihiro, K. Arai[1], H. Takemura, Y. Ochiai, K. Takeuchi and T. Mogami

Silicon Systems Research Laboratories and [1]R&D Technical Support Center, NEC Corporation
1120, Shimokuzawa, Sagamihara, Kanagawa, 229-1198, Japan
Phone: +81-42-779-6193, Fax: +81-42-771-0886, E-mail: s-yamagami@ab.jp.nec.com

1. Introduction

Reduced body effect, negligible junction capacitance, and excellent soft-error immunity make SOI-CMOS devices attractive for low-power, high-speed ULSI circuits applications [1-5]. To simplify the circuit design, reduction of the floating body effect (FBE) is desirable[5]. Fully depleted (FD) SOI-MOSFETs are attractive because the FBE is small. However, if the body-to-source potential barrier remains, the FBE is not completely eliminated even in FD-SOI-MOSFETs. A possible measure against the FBE in FD devices is the use of a body contact structure, which is widely used for partially depleted (PD) SOI-MOSFETs. However, the effectiveness of a body contact in FD-SOI-MOSFETs has not been clearly demonstrated. Furthermore, a new fabrication process to form a body contact in a ultra-thin SOI film is also necessary.

In this work, a body contact structure using elevated field insulator [6] is proposed to maintain the layout-compatibility with bulk design even for ultra-thin SOI films. FBE suppression in FD devices caused by the body-contact is demonstrated. The body bias effect immunity in body contacted FD devices is also discussed.

2. Body Contact Structure

Partial trench isolation [7] is already proposed as body contact structure having layout-compatibility with bulk design. However, it is difficult to apply this structure to thin SOI-MOSFETs, because the reduced SOI thickness under the isolation region increases the body contact resistance (Fig. 1 (a)). If the field oxide (FOX) is formed on top of the SOI film, surface of gate polysilicon is not flat (Fig. 1 (b)). In addition, since the channel stopper ion implantation is not self-aligned, misalignment occurs. Figure 2 shows the schematic illustration of the proposed body-contacted FD SOI-MOSFET. As shown in Fig. 2, the SOI film thickness under the field insulator is the same as in the channel. A flat gate polysilicon surface is achieved by two step gate polysilicon deposition. Channel stopper ion implantation is self-aligned.

3. Fabrication Process

Figure 3 shows schematic process sequence. SOI wafers with 30-nm silicon thickness were used. (a) After channel ion implantation, gate oxynitride was grown. 1st gate polysilicon and SiN were deposited. (b) After etching SiN and polysilicon using a resist mask, self-aligned arsenic was implanted to the SOI layer to reduce the resistance from the body to body contact electrode. (c) After SiO_2 deposition, CMP process was carried out using SiN as the stopper. SiN was removed, and then (d) 2nd polysilicon was deposited. The 1st and the 2nd polysilicon are etched simultaneously to form the gate electrode. (e) Contact hole was opened and arsenic ion was implanted. Cobalt silicidation and interconnect formation followed.

4. Results and Discussion

Figure 4 shows measured dependence of the threshold voltage (V_{TH}) on body voltage (V_{BODY}) for the fabricated pMOSFET. The constant V_{TH} around V_{BODY} = 0 V indicates that the MOSFET is fully depleted. Figures 5 (a) and (b) show the I_D-V_D characteristics of the pMOSFETs with and without the body contact, respectively. The kink observed in Fig. 5 (b) is eliminated by adding a body contact in Fig. 5 (a).

The difference is explained as follows: Even if the operation mode is FD, carriers generated by impact ionization accumulate in the body region (Fig. 6), and causes a shift of the electron quasi Fermi level (It should be noted that V_{BODY} in Fig. 4 corresponds to the electron quasi Fermi potential at the body). In the present device, a Fermi potential shift of 0.3 eV is the critical point for the V_{TH} shift, as shown in Fig. 7. If this shift is lower than 0.3 eV, the floating body effect does not occur.

To evaluate the quasi Fermi level shift in the MOSFET without body contact, the impact ionization current (I_{II}) and the body-to-source diode current (I_{DIODE}) were measured (Fig. 8). If there is not a body contact, the impact ionization current and diode current should balance. Figure 8 shows that a quasi Fermi level shift of 0.55 eV is required to balance these currents at a drain voltage of 1.5V. The value is large enough to cause the floating body effect, as shown in Fig. 7. A curve indicated as "I_{BODY}" in the Fig. 8 shows the measured dependence of body current on E_{Fe} in the body contacted device. Although a FD device does not have a neutral body, I_{BODY} is 2 orders of magnitude larger than I_{DIODE}. At the drain voltage of 1.5 V, quasi Fermi level shift required to balance the impact ionization current is reduced to 0.25 eV, which is smaller than the 0.3 eV limit shown in Fig. 7. The results are consistent with the kink suppression at drain voltage of lower than 1.5 V shown in Fig. 5 (a).

Finally, it should be noted that even if a body contact is used, the drive current degradation due to the body bias effect, which is a drawback for PD devices, is still absent for the FD devices, as can seen from Fig. 4.

5. Conclusions

The body contact structure using elevated field insulator having layout-compatibility with bulk design and suitability for thin SOI film was developed. The body contact operation in FD-SOI-MOSFET was investigated. It was demonstrated that the proposed body contact is effective to suppress the FBE in FD-SOI-MOSFETs.

References

[1] I.Y. Yang, et al., IEDM 1999, p. 431. [2] S.K.H. Fung, et al., IEDM 2001, p. 629. [3] R. Chau, et al., IEDM 2001, p. 621. [4] M. Celik, et al., VLSI Tech. 2002, p. 166. [5] T. Kudo, et al., VLSI Tech. 2002, p. 168. [6] J.-W. Lee, et al., VLSI Tech. 2002, p. 42. [7] Y.Hirano et al., IEDM 2000, p.467.

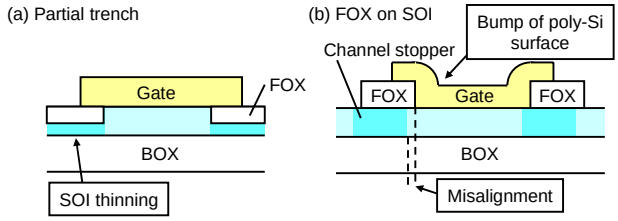

Fig.1 Various conventional body contact structures.

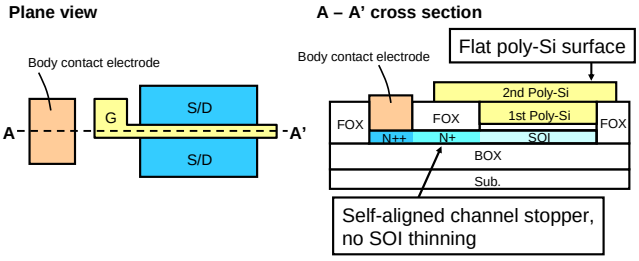

Fig.2 Schematic illustrations of proposed body contact structure using elevated field insulator and two step polysilicon deposition. (pMOS).

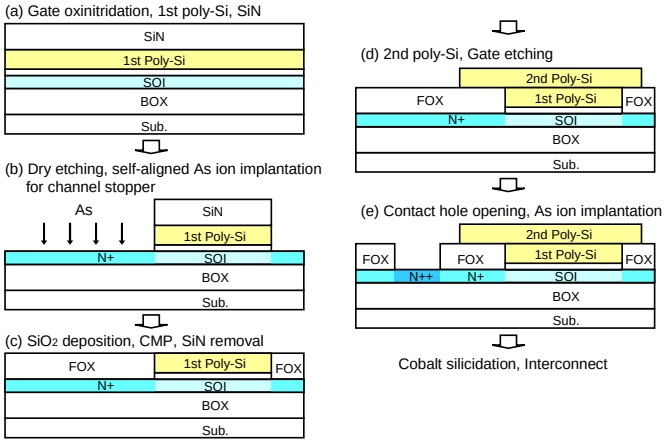

Fig.3 Process sequence of thin-film SOI-pMOSFET with body contact using elevated field insulator.

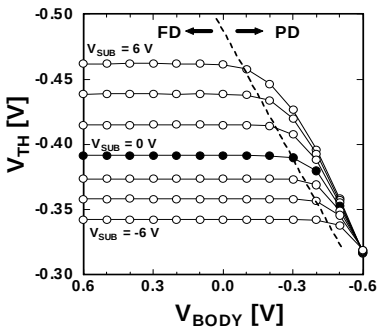

Fig.4 Threshold voltage dependence on body voltage.

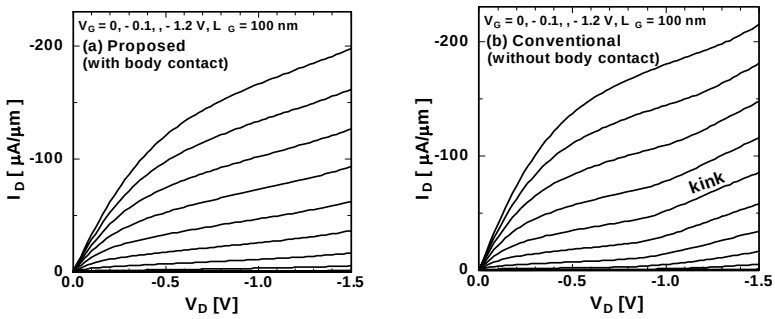

Fig.5 I_D-V_D characteristics of SOI-MOSFET. (a) Proposed (with body contact). (b) Conventional (without body contact).

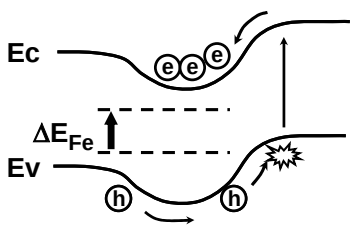

Fig.6 Schematic band diagram of p-MOSFET at the bottom of SOI. ΔE_{Fe} means a shift of the electron quasi Fermi potential.

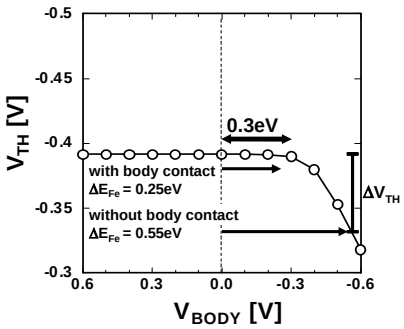

Fig.7 Threshold voltage dependence on body voltage. If variation of body voltage is lower than 0.3eV, threshold voltage is constant.

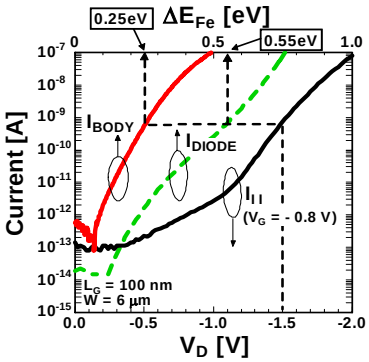

Fig.8 Measured impact ionization current, body-to-source diode current and body current.