

High Performance 45nm CMOS Technology with 20nm Multi-Gate Devices

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1. Introduction

In the 2003 ITRS roadmap all CMOS leakage currents have been scaled down to prevent a power crisis on the circuit level. In order to maintain high performance the target power supply voltage is kept at 1.1V. Further performance enhancements using strained silicon or multiple gates have also been proposed [1-4]. We present a multi-gate device with locally strained channel based on ultra-thin SOI and fully silicided NiSi gate. Device performance ($I_{on}=1.8mA/\mu m$ at $I_{off}=13.3nA/\mu m$ for NMOS and $I_{on}=1.08mA/\mu m$ at $I_{off}=4.9nA/\mu m$ for PMOS) meets the 2003 ITRS roadmap requirements for the 45nm technology node in 2009[5].

2. Device Fabrication

Devices are made using 6-9nm thick silicon on 200nm buried oxide, mesa isolation, oxide/nitride gate stack with EOT=1.3nm, fully silicided gate with 20nm length, 30nm thick selective epi (SEG) in extension and source/drain area (Fig. 1). The channel region remains undoped. The NiSi gate layer has intrinsic tensile stress of 0.9GPa. A 193nm lithography process is used to pattern devices with 5 parallel channels and fan-out source/drain region. The metal gate wraps the channel from three sides and causes high tensile stress in the narrow (<100nm) channel (Fig. 2), while for wide devices a large part of the channel is under compressive stress.

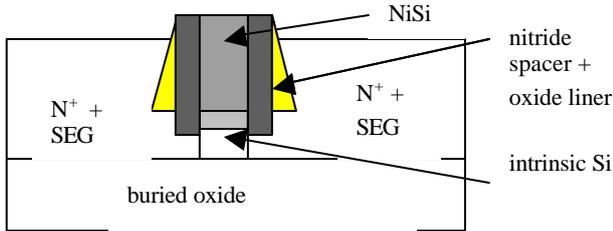


Fig. 1: Ultra-thin FDSOI device with NiSi gate and SEG.

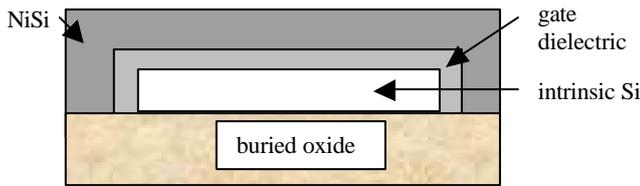


Fig. 2: Cross-section through one channel showing NiSi gate wrapping intrinsic silicon channel from three sides.

3. Device Performance

Fig. 3 shows comparison between wide (2 μm) and multiple-finger devices with top silicon layer width of 65nm (total finger gate width of 80-85nm). The combination of high inversion charge at the sidewalls (electrostatics) and mobility enhancements due to high strain increase drive current by more than 100%. Narrow NMOS devices benefit more from the stress effect as seen in the linear curve in Fig. 3, since mostly compressive stress in wide devices degrades performance. The third benefit is in superior electrostatics control for narrow devices with L~20nm (improved DIBL, off-state leakage, and subthreshold slope,

higher V_0). The multiple-finger design improves parasitic R_{sd} .

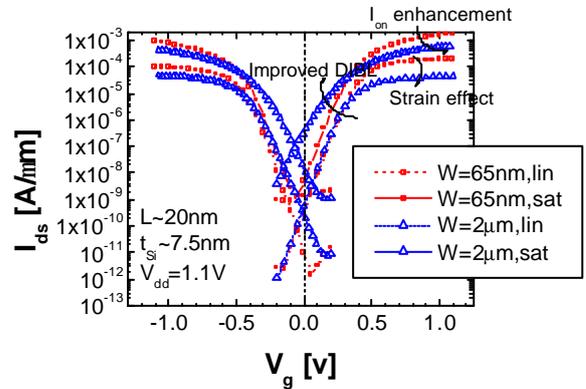


Fig. 3: I_{ds} - V_{gs} curves for 20nm wide (2 μm) and narrow (65nm) NMOS and PMOS devices.

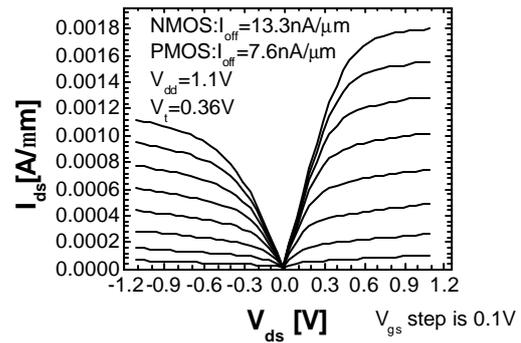


Fig. 4: I_{ds} - V_{ds} curves for 20nm narrow ultra-thin silicon FDSOI devices.

We achieve the highest performance reported with $I_{on}=1.8mA/\mu m$ and $1.08mA/\mu m$ for NMOS and PMOS, respectively (Fig. 4). The resulting intrinsic transistor speed (CV/I) is 0.26 and 0.45ps (shown in Fig. 5), which exceeds preliminary requirements of the 2003 ITRS roadmap. A complete device performance comparison is shown in Table I.

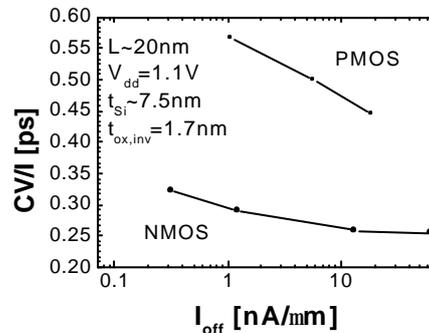


Fig. 5: CV/I vs. off-state leakage for 20nm devices.

Table I: Device performance comparison

Device Parameter	2003 ITRS		This Work	
	NMOS	PMOS	NMOS	PMOS
Lgate [nm]	20	20	20	20
Tox,inv[nm]	1.2	1.2	1.7	1.7
Vdd [V]	1.1	1.1	1.1	1.1
Ioff [nA/ μm]	70	70	13.3	4.9
Ion [mA/ μm]	1.8	0.818	1.802	1.081
Vtsat [V]	0.19	-0.19	0.273	-0.311
S [mV/dec.]	78	78	72.7	71.6
Gm [S/mm]	2.47	1.12	2.728	1.756
jg [A/cm ²]	117	N/A	25	6
CV/I [ps]	0.5	1.1	0.26	0.45

4. Discussion

One of the major concerns of the ultra-thin FDSOI device is the control of silicon thickness [6]. We reported initial results in [7] and with thinner silicon layer and better uniformity across the wafer we observe tighter distributions of threshold voltage, subthreshold slope, and DIBL (Figs. 6,7).

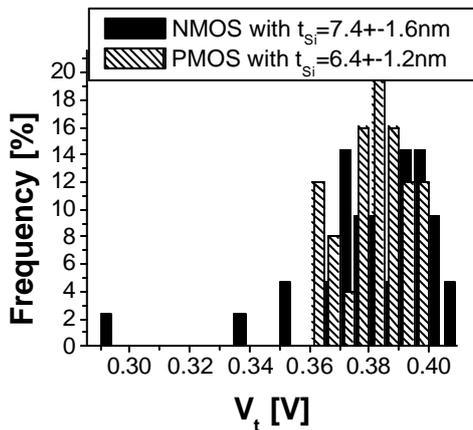


Fig. 6: Threshold voltage distribution for two wafers with different silicon thickness, showing much better control with thinner silicon and smaller standard deviation.

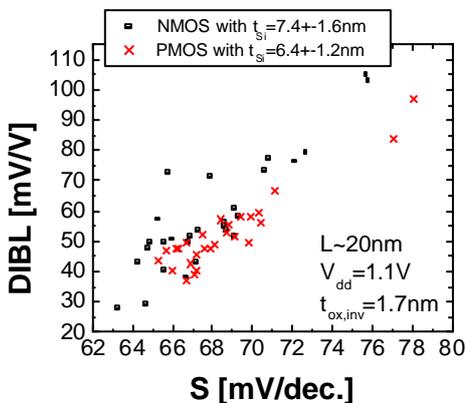


Fig. 7: Thinner silicon layer with better control across the wafer yields tight distributions of S and DIBL.

The main disadvantage of narrow devices is that they are not area efficient for large driver circuits. Although it is predicted that by 2009

high performance microprocessors will use ~80% of the silicon area for cache that uses very narrow devices, using multi-gate devices can impose area penalty for wider transistors. Our narrow devices, using 90nm design rules, also exhibit area penalty (Fig. 8) when comparing them with wide devices with the same off-state leakage. But our process is unique in a way that we can print conventional wide devices without a single additional processing step. Lithography simulations for an advanced 193nm lithography scanner, suitable for the 45nm node, which is expected to be available in 2009, show that much smaller active area pitches will be available, yielding a superior area efficiency of the narrow multi-gate devices (Fig. 9).

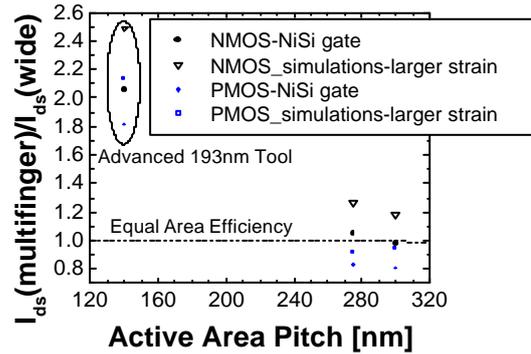


Fig. 8: Area efficiency for multi-finger narrow devices. Full symbols represent experimental data, open symbol represent simulated data assuming larger strain obtained by a different silicidation process.

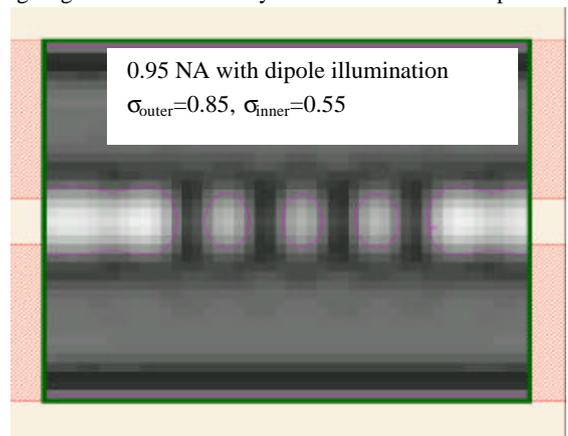


Fig. 9: Lithography simulations of a multi-finger device with finger width of 50nm and finger length of 90nm using an advanced 193nm lithography scanner.

5. Conclusions

We demonstrate experimentally that multi-gate very narrow FDSOI devices with ultra-thin silicon can meet device requirements of the 2003 ITRS roadmap for the high performance 45nm technology node. They are very suitable for locally introduced strain to enhance performance.

References

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