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Double Gate MOSFET by ESS (Empty Space in Silicon) Architecture

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Abstract

Double gate (DG) MOSFET employing ESS (Empty Space in Silicon) architecture exhibited remarkable device characteristics. Significant performance gain was clearly observed comparing to a planer bulk device. This advantage is mainly due to the steep sub-threshold characteristic which is the typical double gate feature. The ESS double gate architecture is fully compatible with current conventional bulk CMOS process. This typical feature could make double gate FET into realistic candidate of next high performance device.

Introduction

FD/DG/GAA-SOI has been discussed as a promising structure for future scaling devices because of the high SCE and DIBL immunity[1-3]. However, complicated integration scheme will be needed to realize such kind of devices. On the other hand, we had developed the new technique to fabricate SON (Silicon on Nothing) structure on bulk substrate, named ESS technique[4-6]. The ESS technique has several advantages; (1) Partial SOI (SON) on bulk substrate: The merit of SOI structure can be utilized on bulk wafer. This is appropriate for System on a Chip (SoC) applications. (2) Simple process: The ESS process needs only the trench fabrication and high temperature annealing. This will produce significant process cost reduction comparing to the use of SOI wafer. (3) Low self-heating: The ESS structure is made at part of active area region. Thus, thermal flux can easily flow into the Si substrate. (4) Free layout: ESS with the arbitrary size and shape can be formed by controlling the initial trench size and layout.

In this paper, distinguished DG FET characteristics will be demonstrated with practical ESS architecture.

DG-ESS FET Process

A simple process sequence of the DG-ESS FET is shown in Fig. 1. First, high aspect ratio trenches were formed at surface of Si wafer. After that, ESS was formed by the trench transformation on high temperature hydrogen annealing. Next, SON thickness was thinned by CMP and oxidation process. Then, flat device surface over the ESS was obtained. STI pattern was aligned with ESS pattern. Conventional CMOS process could be applied after STI process. In this study, HDP-USG (anisotropic deposition property) was used for filling the STI. Thus, the ESS was not filled at STI formation step and a seam was created beside the ESS. As a result, the ESS was filled by polysilicon as a bottom gate electrode at the same time of top gate electrode deposition. The surrounding gate structure was made with this buried polysilicon.

Figure 2 shows the schematic layout of the DG-ESS FET. Pipe-shaped ESS is formed under the top gate and extends to the STI region. Figures 3 and 4 show the TEM image of the A-A' and B-B' cross section of the fabricated DG-ESS FET, respectively. No defect was observed at the channel region and around ESS structure. Also it was confirmed that the thin flat Si layer surrounded by the poly silicon gate could successfully be obtained. In this structure, there is no need to make a contact to bottom gate electrode. The bottom surface of active Si layer was atomically flat due to surface migration. Thus, thickness of active Si layer became quite uniform as can be seen in fig. 4.

Device Characteristics and Discussions

Electrical results of DG-ESS FET were verified comparing to conventional bulk MOSFET, which were fabricated on the same wafer. The size of ESS and the thickness of the active Si layer should be well controlled to enjoy the merits of DG structure. Figure 5 shows the dependence of threshold voltage on substrate voltage at several gate lengths. The body effect coefficient of DG-ESS FET is varying with the change of gate length for a given ESS size. At the short channel region, where the gate length is shorter than the size of ESS, channel region is electrically isolated from the substrate. This device is same as floating body double gate structure. Figure 6 shows ideal subthreshold property at the shortest gate length which is around 0.2μm. On the other hand, in case that gate length is 1.0μm, which is larger than the ESS size, there is no difference in device characteristics at all regardless of ESS. As shown in Figs. 5 and 6, gate length has to be set shorter than ESS size to obtain the merit of floating body double gate device.

Typical Id-Vg and Id-Vd characteristics of DG-ESS FET are shown in figs. 7 and 8, respectively. Steep subthreshold characteristics and higher drive current were observed. Drain current enhancement of DG-ESS FET was successfully achieved by 75% for NMOS and 97% for PMOS comparing to bulk FET which has same device width. On the other hand, the series resistance in the extension region could become important when the gate length becomes much shorter than the ESS size. However, the size of ESS is well controllable for each gate length.

Finally, self-heating effect, which is one of critical issues of SOI device, was simulated using SON FET structure. The lattice temperature distribution due to self-heating was simulated as shown in Fig. 9 for conventional SOI FET(left) and SON FET(right). The better heat dissipation was clearly confirmed on SON FET since there is no insulator under source and drain region. DG-ESS FET shows more better heat dissipation than SON FET because SON region is filled with silicon, which has 100x lower thermal resistance compare to buried oxide.

Conclusions

DG-ESS FET was successfully realized by using ESS technique. DG-ESS FET shows the high drivability and good subthreshold property. Simple process sequence for making DG device has been demonstrated, which is compatible with conventional CMOS process. As a result, this novel scheme can fabricate both double gate and conventional device on the same wafer without any performance degradation. These results suggest that DG devices using ESS architecture is appropriate for SoC applications, due to the merit that DG structure can be fabricated partially on bulk substrate.

References

1) J. P. Colinge et al., SSDM Tech. Dig., p.238, 2001.
2) D. Hisamoto, IEDM Tech. Dig., p.429, 2001.
3) S. Monfray et al., VLSI Tech. Dig., p.108, 2002.
4) T. Sato et al., IEDM Tech. Dig., p.517, 1999.
5) I. Mizushima et al., Appl. Phys. Lett., **77**, p.3290, 2000.
6) T. Sato et al., IEDM Tech. Dig., p.809, 2001.

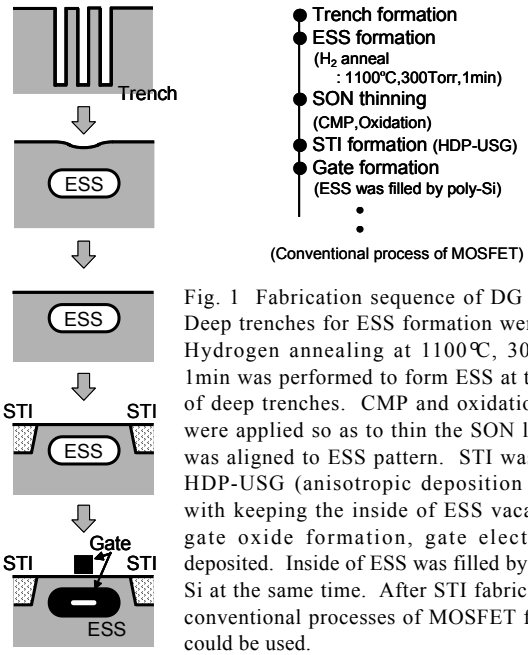

Fig. 1 Fabrication sequence of DG ESS FET. Deep trenches for ESS formation were formed. Hydrogen annealing at 1100℃, 300Torr for 1min was performed to form ESS at the bottom of deep trenches. CMP and oxidation process were applied so as to thin the SON layer. STI was aligned to ESS pattern. STI was filled by HDP-USG (anisotropic deposition property) with keeping the inside of ESS vacant. After gate oxide formation, gate electrode was deposited. Inside of ESS was filled by gate poly-Si at the same time. After STI fabrication step, conventional processes of MOSFET fabrication could be used.

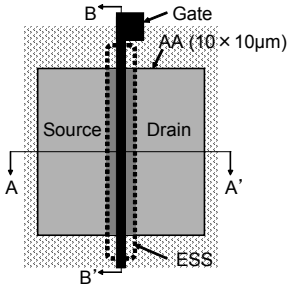

Fig. 2 Schematic layout of the fabricated DG-ESS FET. Pipe-shaped ESS was fabricated under the gate electrode, which was larger than the width of active area region. Inside of this pipe-shaped ESS was filled by the gate poly-Si.

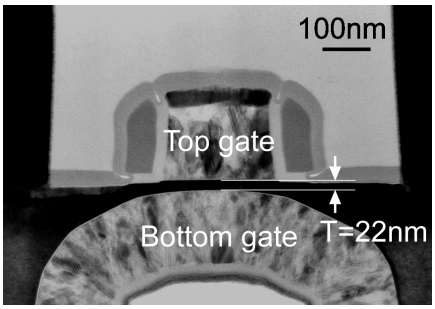

Fig. 3 A-A′cross sectional TEM image of the fabricated DG-ESS FET. The thickness of active silicon layer was 22nm. Gate length was 0.2μm. Inside of ESS was filled with the gate polysilicon.

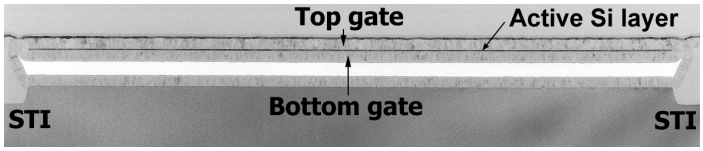

Fig. 4 B-B′cross sectional TEM image of the fabricated DG-ESS FET. The thin and uniform active silicon layer could successfully be obtained. Channel width was 10μm. The thickness of active silicon layer was 22nm.

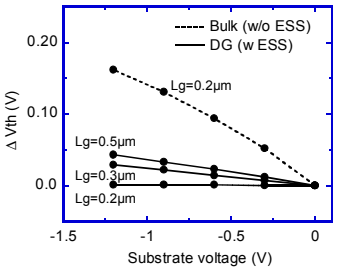

Fig. 5 Substrate voltage dependence of subthreshold characteristics with gate length as a parameter. When a -1.2V substrate bias was applied to the bulk device, more than 0.15V increase of threshold voltage was observed. Under the same bias condition, the threshold voltage of DG-ESS FET did not increase at all when the gate length is less than 0.2μm. This means that the channel region is fully isolated from the substrate by ESS. The body effect depends on gate length and the size of ESS. The body effect is reduced when the gate length is smaller than the size of ESS.

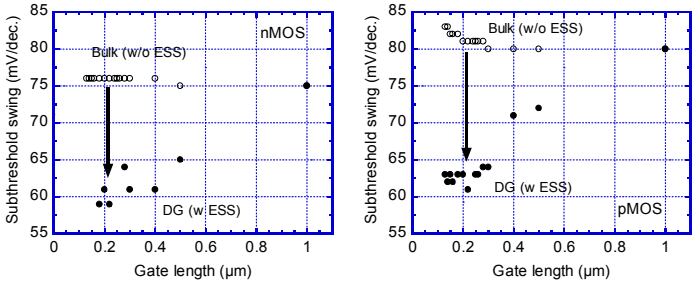

Fig. 6 Gate length dependence of subthreshold swing. Comparison between DG-ESS FET (w ESS) and conventional bulk FET (w/o ESS) are shown for NMOS (left) and PMOS (right). At Lg=1.0um, there was no difference regardless of ESS. Subthreshold swing was drastically improved to about 60mV/dec. for both nMOS and pMOS as the gate length become small.

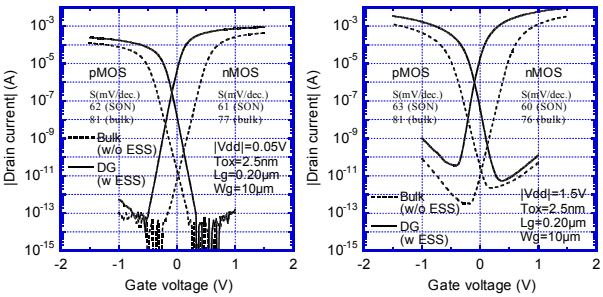

Fig. 7 Measured Id-Vg characteristics of DG-ESS FET (w ESS) and conventional bulk FET (w/o ESS) for |Vdd|=0.05V (left) and |Vdd|=1.5V (right). The thickness of active silicon layer was 22nm. Steep subthreshold property was observed.

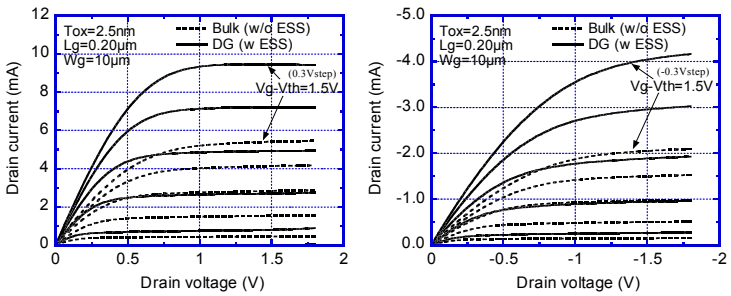

Fig. 8 Measured Id-Vd characteristics of DG-ESS FET (w ESS) and conventional bulk FET (w/o ESS) for NMOS (left) and PMOS (right). Drastical drive current increase was confirmed on DG-ESS FET. (75% for NMOS and 97% for PMOS)

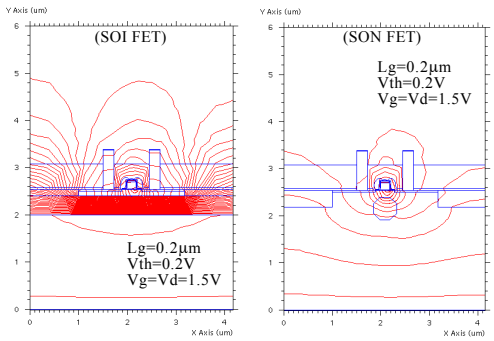

Fig. 9 Self-heating effect was simulated on SON FET compared with SOI FET. Temperature increase at the channel region was much reduced on SON FET, which has the heat dissipation pass to the substrate at S/D region. Drain current reduction due to the self heating was estimated 3.2% for SON FET compared with 9.5% for SOI FET.