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Novel Capacitor Structure Using Sidewall Spacer for Highly Reliable FRAM Device

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1. Introduction

Recently, numerous researches and developments were focused on developing high-density ferroelectric devices for stand-alone or embedded memory applications due to their ideal memory properties.[1,2] Current high-density ferroelectric devices are typically fabricated by 1T1C cell architecture and COB cell structure for enhancing cell efficiency and cost effectiveness. In particular, the ferroelectric capacitor should be patterned in given small cell area, which can be achieved by 1 mask etching process with high etching slope. Even though the capacitor etching technology is a simple and efficient process, it is very difficult to establish the 1 mask etching process without an undesired etching damage to the ferroelectric capacitor, which induces low remnant polarization and thus degrades the reliability property.[3] Therefore, in this study we thoroughly investigated the origin of the degradation of the 1 mask etched ferroelectric capacitor, and proposed a novel capacitor formation technology to eliminate the etch-induced degradation.

2. The Origin of Degradation of Ferroelectric Property in the Stacked Capacitor Structure

Figure 1 shows the 2Pr value of the $Pb(Zr_x,Ti_{1-x})O_3$ (PZT) capacitors measured at 85°C as a function of applied voltage for two ferroelectric capacitors with different sizes of 6.44×6.44μm^2 and 0.48×0.92μm^2, respectively. The size of small capacitor is equivalent to real capacitor size of memory cell of FRAM device.[1] The 2Pr value of real memory cell capacitor is about 30% lower than that of the large capacitor. This discrepancy can be explained by the portion of perimeter and area region (perimeter factor) of the capacitor. The perimeter factor of large capacitor is 0.09 and that of capacitor of memory cell is 0.95. The larger the perimeter factor, the lower remnant polarization value. This implies the sidewall of the ferroelectric capacitor etched by 1 mask is closely correlated with the degradation of ferroelectric property.

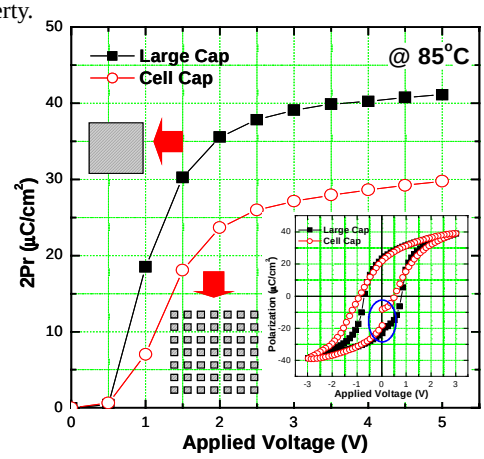

Figure 1. The remnant polarization of large capacitor and small capacitor as a function of applied voltage.

In order to find out exact process step responsible for the degradation, we prepared two kinds of ferroelectric capacitor. One sample is the fully etched capacitor with 1 mask, and the other is the capacitor with un-etched bottom electrode (BE). The remnant polarization value of the fully etched capacitor was 78% of that of the capacitor with un-etched BE, as illustrated in Figure 2. This indicates that the major degradation of ferroelectric property is caused by the BE etching process.

The effect of the BE etching process on the PZT film was systematically investigated. Figure 3 shows the conventional stacked capacitor etched with 1 mask. The sidewall of PZT film was exposed to BE etching environment during the BE etching process. The crystallinity and compositions of sidewall of PZT film after BE etching process was evaluated by preparing the PZT films exposed to the BE etching gas chemistry. It was observed in Figure 4 that the surface became very flattened with no grain topology.

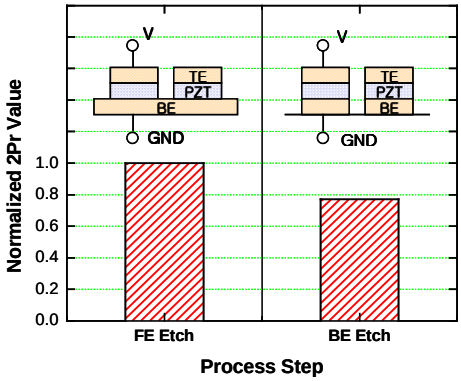

Figure 2. The remnant polarization as a function of process step.

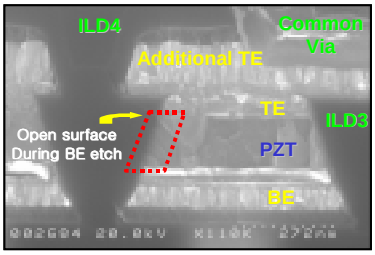

Figure 3. SEM profile of the conventional stacked capacitor etched with 1 mask.

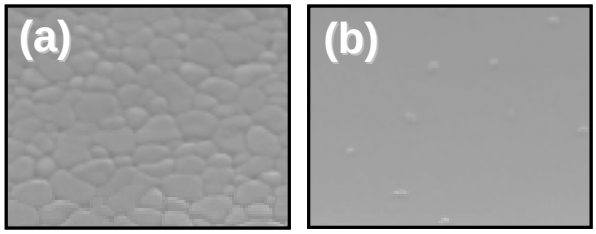

Figure 4. Surface morphology of PZT surface. (a) As-grown PZT film (b) PZT film exposed to BE etching environment

X-ray diffraction (XRD) pattern was investigated as illustrated in Figure 5 for the PZT films exposed to the BE etching environment. It was found that (111) peak of perovskite structure was appreciably reduced, though there are no significant changes of the film thickness. The changes of surface compositions of the PZT film exposed in BE etching environment are shown in Figure 6. The distinguishing feature of compositions was the loss of Pb element. The ratio of Pb/(Zr+Ti) is below 0.6 at the surface whose value is gradually increased as the depth is increased. From the surface analysis of the PZT films, it was found that the PZT film became Pb-deficient and seemed to be amorphorized by the BE etching environment. This Pb-deficient and amorphorized layer

might be the origin of remnant polarization loss. Switched polarization is easily relaxed when the non-stoichiometric layer existed on the sidewall. The depolarization phenomenon ($P_r^{\wedge}$) was clearly observed in the inset of Figure 1, which the starting point was widely displaced from ending point of hysteresis loop.

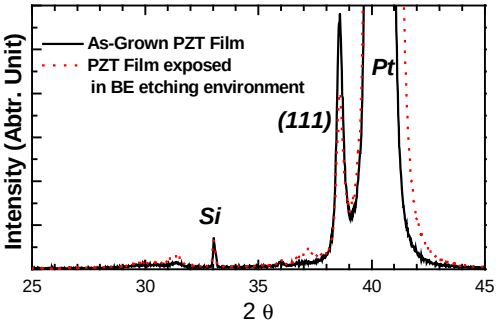

Figure 5. XRD patterns of as-grown PZT film and PZT film exposed to BE etching environment.

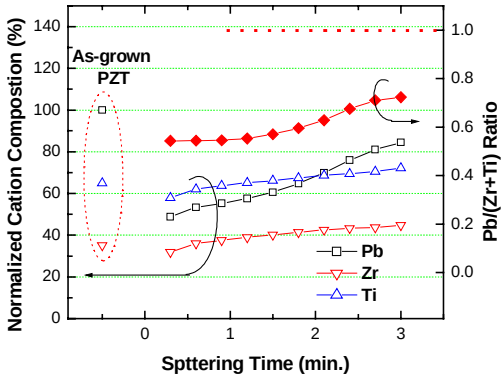

Figure 6. Depth profile of composition and Pb/(Zr+Ti) ratio of PZT film exposed to BE etching environment.

3. Novel Capacitor Etching with Spacer

In order to prevent the undesired layer induced by the BE etching process, we proposed a novel capacitor etching scheme using "ferroelectric (FE) sidewall spacer". The FE sidewall spacer can protect a chemical attack during the BE etching process as well as behave as an etch mask. Figure 7 shows the sequences of the capacitor etching process using the FE sidewall spacer. First of all, the capacitor was etched to the ferroelectric film as usual, and then an insulating layer was deposited with adequate thickness on the FE-etched capacitor as shown in Figure 7 (a). Then, etch-back process was carried out for the formation of FE sidewall spacer as shown in Figure 7 (b). Finally, the BE etching process was performed on the ferroelectric capacitor with FE sidewall spacer. There are two critical points for selecting the sidewall spacer. The insulator should be compatible to the ferroelectric material and also have high etching selectivity over BE noble metals. The compatibility means that the insulator should not degrade the ferroelectric property by reacting with ferroelectric films during deposition. The high etching selectivity makes it possible that the insulator remained after completing the BE etch process.

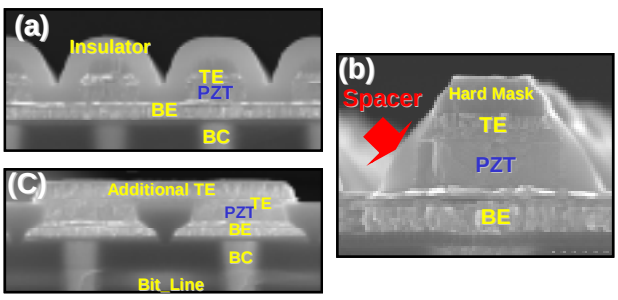

Figure 7. The sequences of capacitor etching scheme using FE sidewall spacer. (a) insulator deposition after FE etching (b) spacer formation (c) BE etching and additional TE formation

Figure 8 shows the comparison of remnant polarization between the memory cell capacitor etched by FE sidewall spacer and the conventionally etched capacitor of memory cell. Even though the remnant polarization value of the novel capacitor is not exactly matched with that of large capacitor, the value was drastically improved by 30% at 3.0V, compared with that of conventionally etched capacitor. As shown in the inset of Figure 8, the $P_r^{\wedge}$ value of the novel capacitor was greatly reduced, indicating that the depolarization phenomenon is effectively improved by novel FE sidewall spacer scheme. This increase of remnant polarization leads to the large sensing margin of 32M FRAM device as shown in Figure 9. Bit-line developed voltage (V_{bl}) was increased to 600mV for the data "1" and was decreased to about 200mV for the data "0", resulting in large sensing margin of 400mV. This large sensing margin is very crucial for the retention property of ferroelectric device.

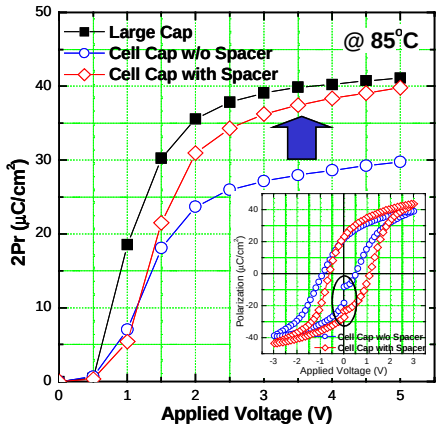

Figure 8. The remnant polarization of the capacitor etched with FE sidewall spacer and the conventional capacitor etched with 1 mask.

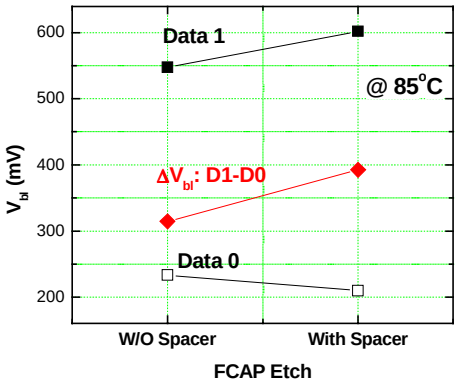

Figure 9. The sensing margin of 32M FRAM with the capacitor etched with FE sidewall spacer and the capacitor conventionally etched with 1 mask.

4. Summary

It was found that the degradation of small cell size capacitor was originated from the formation the non-stoichiometric and amorphorized PZT layer on the sidewall of PZT film during BE etching process. The undesired degradation was greatly reduced by developing the novel capacitor etching process using FE sidewall spacer. The sensing margin of FRAM device, which is very crucial in retention property, was drastically improved by capacitor etch scheme using FE sidewall spacer. It was demonstrated that highly reliable FRAM device is realized by developing the capacitor with FE sidewall spacer.

References

[1] H. H Kim, et al., Symp. on VLSI Tech. Dig., p. 210, 2002.
[2] T. S. Moise, et al, Tech. Dig. IEDM, p. 535, 2002.
[3] Y. J Song, et al, VLSI Tech. Symp., 2003. (to be appeared)