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Floating gate type nonvolatile memory reliability issues

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1. Introduction

Floating Gate (FG) type Non-Volatile Memories (NVM) are currently the standard ones in nearly all NVM technologies. They are widely used either as stand-alone memories (FLASH, EEPROMs) or as embedded memories (Smartcards, µC). Per definition these NVMs are non-volatile and they should not loose their content after power off. But the real world is not perfect. Unfortunately, the time-constants of charge leakage are extremely long. Besides data-retention there are more reliability topics in these NVMs. This article will cover a few of them.

2. Failure modes and testing

NVMs suffer from different failure modes. The table 1 summarizes the most dominant ones.

In best case every unreliable cell would be detected during the regular testing at the end of silicon processing or maybe at packaged devices. But unfortunately, a few of these failure modes have an erratic characteristics which means that every cell can be affected and one cannot determine the failing cycle or failing time during operation. Also the acceleration of some failure modes is not reasonable although it is possible in principle. Furthermore, some failure modes are linked, as shown later. In this sense it is mandatory to take care of the right test flow sequence.

On the other hand related to this is the quality check of an existing or modified test program. This learning is the content of this publication. We defined a standardized specific test flow for a quality measure of existing silicon. This Confidence Level Test (CLT) takes care of some general observations on fail bits (fig. 1). Although this approach is time consuming we get reliable specific failure mode rates at the end. The CLT can be used either on wafer level or on packaged devices, but always only on "good dies" after standard test. This method allows a quality check of silicon processing issues or process changes, or of test flow modifications in FEOL or BEOL and etc.. Also the monitoring of production quality is possible.

The first test determines the Disturb Bit (DB) sensitivity of the material. This sensitivity is related to technology and circuit design. Some processes show a distinct increase of this DB failure rate.

The second test checks the Write/Erase (W/E) sensitivity up to the worst-case conditions for program-code applications in embedded NVM applications. Nowadays due to intelligent programming algorithms on chip only extrinsic early failures will be detected. But this cycling stresses the cells and generates data retention fails additionally.

The third test was described in detail in ref.1. The goal of this test is to get the Erratic Bit (EB) failure rate and to stress the samples for the later Moving Bit (MB) search in the last tests.

Besides these tests the endurance (maximum of W/E cycles until first fail) will be regularly checked and analog measurements (read-disturb, MBs) are done regularly.

Using this test methodology general behaviors can be observed. A few of them will be briefly described which have been found in our 0.22 –0.65µm eFlash technologies. Figure 2 shows a strong correlation between the DB and EB failure rates, which can be physically understood. On the other hand there is clearly no correlation of DBs with "Moving Bits" MB (fig.3). Therefore an independent measure on MB rate is mandatory.

	Observation / Features	**Physical Route Cause**	**Accelerators**
Erratic Bit (**EB**)	Erratic Programming: unpredictable, random, not screen-able, not stable, every cell can be affected	cluster of positive charges by hole injection (GIDL or AHI)	Eox (TOX electric field)
Disturb Bit (**DB**)	Distinct Vth shift of unsel. cells during program.: unpredictable, random, high temperature healing, every cell can be affected in principle	trapped single holes @ Coloumb Barrier Lowering (CBL) enhances FN-tunneling	Eox
Data Retention Bit (**DR**)	Charge Loss after high temperature anneal	defects in isolation oxides, ions	temperature
Moving Bit (**MB**)	Charge Loss at room temperature, Leakage path healed at high temperatures	trap assisted tunneling (TAT)	Eox
Read Disturb 1 (**RDL**)	Charge Loss during long time operation	field enhanced charge loss due to TAT or CBL	Eox
Read Disturb 2 (**RDG**)	Charge gain during long time operation	CHE injection during read access	V_{BL}, V_{WL}
Endurance Fails (**EN**)	No more WRITE or ERASE after several W/E cycles	charge trapping in TOX or TOX breakdown	Eox

Table 1: Most dominant failure modes in NVM with Floating Gates as storage node

	Test-Flow	Comment
Test GD	Read “0” margins Mx ERASE (“0”) **GD & DD** Read “0” margins Mx	check DUTs **DB** rate (margin dep.)
	Bake	healing of trap. charges
Test WE	Read “0” margins Mx **n times W/E** **GD & DD** Read “0” margins Mx	generate **DR** (W/E cyc.) **DB**'s rate @ W/E cyc.
	Bake	check DR
Test EB	Read “0” margins Mx **100x (E)STF** Read “0” margins Mx	**DR** fails @ W/E cyc. generate trap. holes **DB** rate @ **EB** rate.
	RT storage 2^n weeks	
Test MB	Read “0” margins Mx	**MB**-rate

Figure 1: Confidence Level Test (CLT) test flow to determine specific NVM failure rates

In general it is possible to accelerate MBs by a negative Control-Gate (CG) voltage. Analog measurements can simply detect MBs as shown in figure 4. At higher CG voltages (corresponding to higher internal field E_{OX}) a mixture of MB, DB and EB happens and therefore the correlation is lost (fig.3). Figure 5 shows one general problem of MB detection: even MBs are erratic! Not all MB addresses can be reproduced from test to test. Although the statistic is poor one can estimate an acceleration factor of 1-2 decades per MV/cm increase of E_{OX}.

3. Conclusions

A method of checking the reliability related failure rates of NVMs and some observations have been presented. The erratic characteristic of dominant failing mechanisms makes it impossible to screen these weak cells and only a failing rate can be determined.

Acknowledgements

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References

[1] G.Tempel et al. *Non-Volatile Semiconductor Memory Workshop , Monterey, CA (2003), pp.78.*

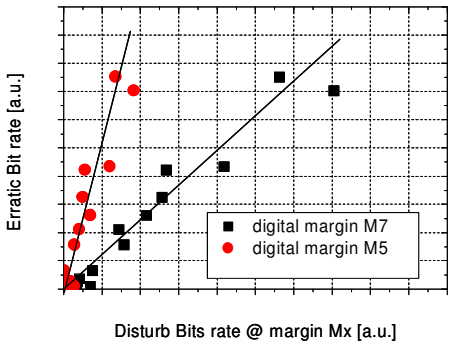

Figure 2: Correlation of Erratic Bit (EB) rate with Disturb Bit (DB) rate, measured at different digital sensing levels Mx

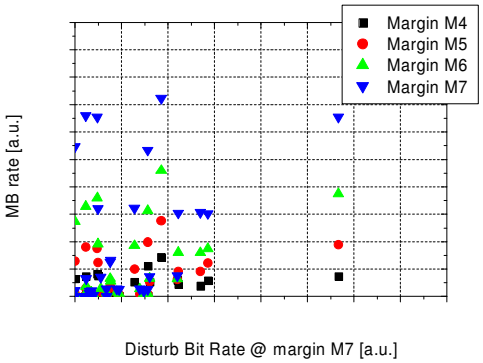

Figure 3:The Moving Bit (MB) rate shows no correlation with Disturb Bit rate independent of sensing level

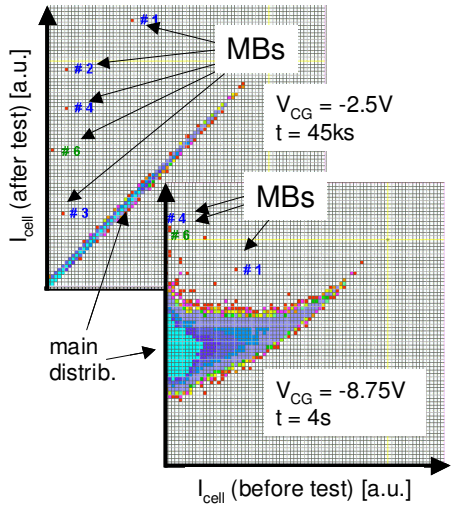

Figure 4: top: analog cell current measurements demonstrate the field acceleration of Moving Bits (MB); bottom: high internal electrical fields generate a lot of additional Disturb Bits etc.

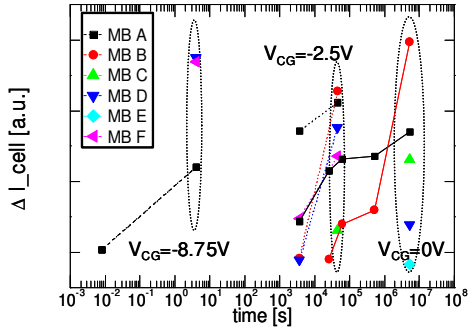

Figure 5:Acceleration of identified MBs with neg. electrical fields