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The Prospect of New Emerging Memories
(invited paper)

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Recently new memory devices such as FRAM, MRAM, PRAM and other new memories have been actively developed to overcome the limit of conventional devices, but it is not clear of the future trends and commercial markets of theses emerging new memories. In this paper, the prospect of new memories will be discussed by comparing the characteristics of new memories and reviewing the current applications of memories for IT products.

1. Introduction

Recently new emerging memories are highlighted due to their possibilities to overcome the limit of conventional memory devices such as, DRAM, SRAM and Flash. These conventional memories have been developed successfully to their own directions of density, speed, non-volatility and cost effectiveness. However there are many questions that this trend can be maintained in the future nano era. Though it is difficult to predict exactly that when do conventional memories meet the scaling limit, we know that it will happen in near future. This uncertain future of these conventional memories makes many researchers and companies develop new memories that will have more scalability, less technical barrier and better properties to pursue universal memory characteristics such as non-volatility, high density, high speed and low power. FRAM (Ferroelectric RAM), MRAM (Magnetoresistive RAM) and PRAM(Phase-change RAM) have appeared to be promising candidates, although their characteristics and technical barriers are not fully understood. Furthermore, to overcome the scaling limit of silicon-based devices, nano-scaled devices such as SET(Single Electron Transistor)memory, Carbon nano-tube and molecular memory have become important research topics. However non-Si based memories are far from the commercial market. Therefore si-based emerging memories such as FRAM, MRAM and PRAM will be concerned in this work.

In this paper, the properties and applications of new memories will be mainly discussed. The key technical issues and directions will be also suggested.

2. New Memories

The main key factor of new memories to have competitiveness over conventional memories is the scalability. So, investigating whether the own characteristics of new memories maintain or not in smaller cell size is one of the best ways to prospect the future of new memories. The scalability and technical barriers for emerging memories will be investigated .

Scaling issues and key technologies of FRAM

FRAM is operated by changing remnant polarization state of ferroelectric material, of which structure is very similar to that of DRAM except for capacitor material. In order to achieve smaller cell size, FRAM cell has been evolved from planar cell to recent COB type stack cell of which ideal cell size factor is 6~8F2. Recent achievement of innovative technology makes the cell size factor be 15F2, as shown in fig.1, which is not small enough comparing DRAM and Flash memory[1]. The major scaling barrier of FRAM is the decrease of remnant poalrization, which corresponds to sensing signal and degradation of reliability in smaller cell size and thinner ferromagnetic material. A 3D cell architecture for future FRAM, as shown in fig.2, leads FRAM cell size factor 6~8F2. In order to achieve a 3D cell structure, ferroelectric capacitor technologies for nano-scaled thin film ferroelectric material and metallic electrode have to be realized. The most critical problem in scaling down FRAM will be arisen from the requirements of reliability, long retention time over 10years at 85 ^{o}C and higher endurance over 10^{14}cycles. In spite of rapid improvement of reliability by adopting MOCVD technology and new material such as Doped PZT and BLT, we do not have a decisive conclusion whether these are sufficient enough for guaranteeing nano-scale ferroelectric capacitor. As a result, it can be concluded that the technology scaling of future FRAM is limited by the ferroelectric film itself whose primary requirement in nano era is the lowest possible film thickness with highest available remnant polarization charge. Unfortunately, none of the known ferroelectric materials can satisfy the requirements in nano era. New growth techniques to improve the known ferroelectric materials and new ferroelectrics are important and necessary for developing FRAM in nano era.

Scaling issues and key technologies of MRAM

The operation of MRAM is to utilize the change of MTJ(Magnetic Tunnel Junction) resistance, which is determined by the relative directions of two ferromagnetic layers[2]. Fig.3 shows the cell architecture of MRAM and MTJ structure of which each layers are ultra thin ranging from several angstrum to several hundred angstrum. The main advantage of MRAM is the high-speed operation and good reliability. The switching speed of the cell is under 6ns and the endurance is also over 10^{8} cycles, of which number does not mean the limit of endurance, but just test time limit in our test environment. There are several technical barriers to scale down MRAM. The first limitation is small sensing signal. The current MR ratio is typically 30% of its resistance, even rapidly improved, so the sensing signal margin is very small. And the more

critical factor is its large variation because the thin tunneling oxide (around 1nm) is exceptionally sensitive to oxide thickness variation and is very susceptible to the process-induced damages such as etching, cleaning and following heat, which will make it difficult to get yield and mass production. This problem will be more severe as MRAM shrinks. The second limitation is the writing disturbance which means a selected MTJ placed at cross point of selected bit-line and digit-line during writing operation disturbs adjacent MTJs resulting in false states. Large variation of switching field of MTJ can cause disturbance problem. The optimization of MTJ shape, aspect ratio, free layer magnetization and the thickness is required to minimize the switching field variations. The third limitation is large writing current. Large writing current causes the increase in power consumption, the increase in chip size and the reliability issues arising from the electro-migration phenomenon in the metal lines. The writing current can be reduced with using magnetic flux concentrating structures in digit-line and bit-lines and optimization of MTJ magnetic properties. However, well-known phenomenon of "the smaller the MTJ dimension, the higher switching field" hinders MRAM technology scaling. Considering all of the technical barriers and technology scaling issues leads us to conclude that MRAM has low expectation to be the main stream memory in nano era. The appealing properties of both fast writing and fast reading speed of MRAM are expected to be used in SOC chips which will be prevalent in nano era.

Scaling issues and key technologies of PRAM

The main mechanism of PRAM is to store two different resistance states that are switched by current induced heat. This device usually uses GeSbTe alloys and it has rapid response and excellent reversibility. The process of PRAM is very compatible to the conventional Si process. Fig.4 presents the I-V curve of PRAM the resistance ratio is larger than 10 that can give large sensing signal margin. And we can also find that the reset current over 1.5mA is required to make amorphous state. This large reset current is the major reason of the difficulty in reducing the cell size, which requires over 2um width of cell transistor with high performance process. Therefore, the reduction of the reset current is the key success factor for achieving high density PRAM and following technology scaling into the nano era. Fortunately the smaller scaling in PRAM can decrease the program volume so that it may reduce the reset current and increase reliability and speed. If high-density process reducing reset current is properly obtained, for example 0.2mA for 256Mb density, PRAM will be good candidate for high-density memory applications comparing other new memories. Also the preliminary evaluation on reliability of PRAM,i.e.2 years of retention at 85°C and over 10^{10} of endurance, does not indicate any inferior characteristics compared to other new memories. If we can reduce reset current with the proper design of cell structure and GST characteristics, PRAM should be expected to be promising memory in nano era [3,4]

Other new memories

Polymer FRAM, RRAM, STTM, PMC and Quantum Dot are also actively studied, but the performance of these devices are still far from matured level, nevertheless, we should not neglect the potential of their application.

3. Characteristics and applications of new Memories

The characteristics of conventional and new memory devices are summarized in Table1 and more visualized diagram is shown in fig.4. These memories have their own advantages, so they are being used for their special application or potentially will be applied for their special field. MRAM and FRAM are non-volatile and high-speed device but scalability is relatively limited. PRAM needs quite large reset current, but it can be reduced with decreasing cell size. Therefore PRAM has the high potential of the high-density and non-volatile device which may compete with Flash. However, conventional DRAM or high speed SRAM may be still major devices in their own field. Considering the application of new memories, the non-volatile memory is the most probable field. Compared to Flash, new memory devices will be used for high performance DSC (Digital Still Camera) which requires much higher speed than Flash. They also have high reliability and non-volatility so that it will be used for mobile phone and PDA that demand low stand-by current. If they are developed for the high density devices, they will be considered as universal memories, which has Flash and DRAM performance at the same time. They can also realize instant-on function that was not possible in Flash. The other strong point of new memories such as FRAM, MRAM, and PRAM are compatible with logic process and electrical characteristics. New devices adopt the simple process so that the embedded memory can be realized with only 2~3 additional masks. Fig.5 shows that SMART CARD with new memory combining EEPROM, SRAM, and MASK ROM can reduce the cost. The new memory embedded SMART CARD has higher speed and more reliable than conventional device has. This device also combines all kind of memory functions so it will improve the effectiveness of memory and software application because of the excellent flexibility.

4. Conclusion

In order to overcome the limit of conventional memories, many kinds of new memory devices are studied, but the universal memory that combines all kinds of memory application has not been yet developed. Especially high-density realization is the major obstacle to replace DRAM and NAND Flash. Therefore, new memories have much difficulty to share large portion of conventional memory market, so they should be developed in the direction of their own strong application fields. The future of new emerging memory mostly depends on how far we can keep its key attributes (ferroelectric capacitor in FRAM, MTJ in MRAM, reset current in PRAM) properly working

5. References

[1] S.Y. Lee and Kinam Kim, IEDM Tech. Dig., p.547 (2002).
[2] M. Durlam et al., Symp. on VLSI Circuits, p.158 (2002)
[3] M. Gill et al., ISSCC Digest of Tech. Papers p.202(2002)
[4] Y.N. Hwang et al., , Symp. on VLSI Tech (2003)

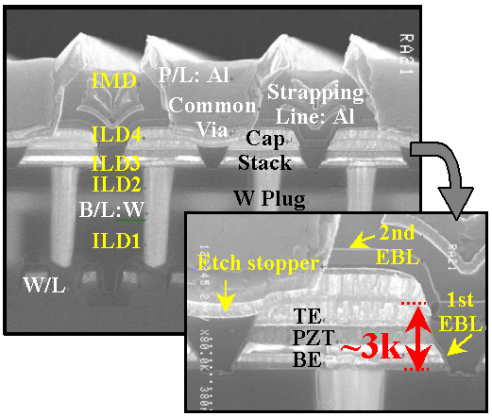

Fig.1 Cross-sectional view of unit cell of 1T1C 32Mb FRAM

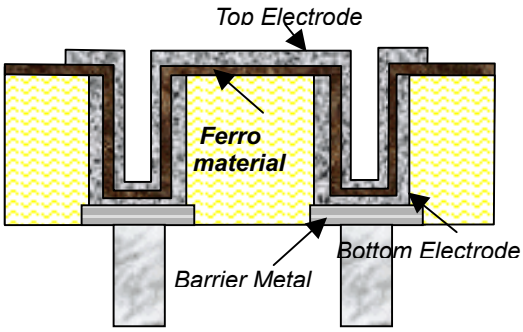

Fig.2 Schematic vertical structures of 3 dimensional cell FRAM

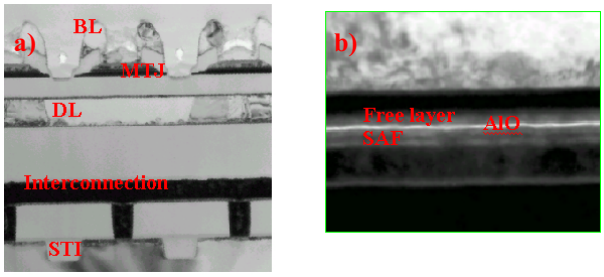

Fig.3 a) Fully integrated MRAM Cell architecture and b) MTJ structure.

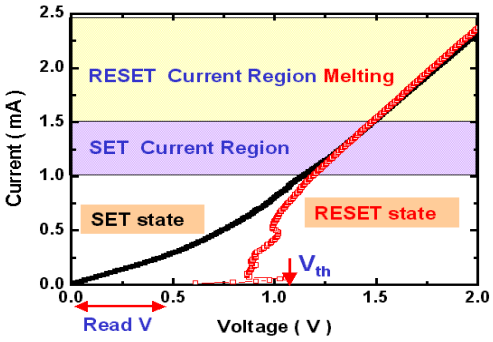

Fig. 4 I-V Characteristics of PRAM Cell. The range of reading is from 0.1V to 0.5V

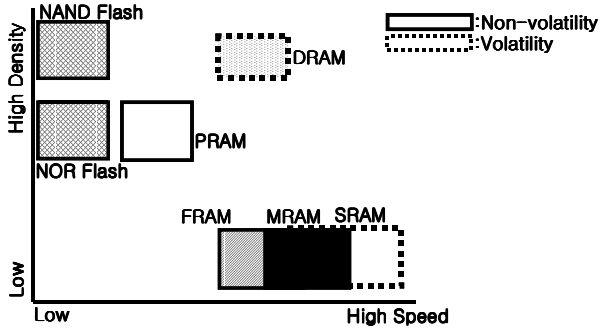

Fig. 5 Characteristics diagram of memories.

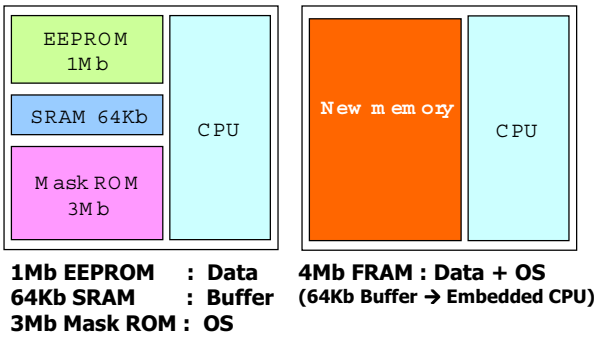

Fig. 6 New memory as a embedded solution. a) conventional SMART CARD b) new memory embedded SMART CARD

	DRAM	SRAM	Flash	FRAM	MRAM	PRAM	Polymer
Non-Volatility	No	No	Yes	Yes	Yes	Yes	Yes
Ideal Cell Size	6F2	50F2	4F2(NAND) 6F2(NOR)	6~8F2	20F2	6~8F2	6F2
Cell Size	8~10F2	50~80F2	5~10F2	15~30F2	>30F2	8~10F2	5~8F2
Scalability	Good	Worst	Good	Bad	Worse	Good	Good
Scalability Limit	Cell Tr. Capacitor	Cell Size	Disturbance Retention	Polarization	Disurbance Switching Current	Reset Current	N.A.
Stand-by Current	~mA	0.1~10mA	20~100uA	<10uA	<10uA	<10uA	N.A.
Sensing Signal	~100mV	~100mV	~10000R	~200mV	~0.3R	10~100R	N.A.
Write Speed	<100ns	<50ns	10us(program) 1ms(Erase)	<100ns	<50ns	<500ns	10us
Read Speed	<100ns		<100ns	<100ns	<50ns	<100ns	10us
Manufactuability SVP* Critical Process	~10% Cap.Dielectric Thickness	<10% Tr. CD	~10% Cell Width Etox	~20% Capacitor Size	~100% Tunnel Oxide Thickness	<10% Contact Size	N.A.
Degradation	-	-	Vth Shift	Polarization	Mn Diffusion	-	Polarization
Endurance	10E15	10E15	10E5	> 10E10	>10E10	>10E10	>10E10
Retention @85C	Volatile	Volatile	10yrs	10yrs	10yrs	10yrs	10yrs

Table.1 Comparison table of memories. Values of new memories are expected based on current technology trend. SVP is the abbevation of "Signal Variation with Process Margin" which means the change of signal due to the 10% change of critical process.