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A 0.18-μm Embedded MNOS-Type Non-volatile Memory for High-Frequency and Low-Voltage Operation

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Abstract

We have developed 0.18-μm embedded split-gate-type MNOS memory for high-frequency operation and low-cost mass production. The thin gate oxide of the control-gate MOS device makes it drivable by a fine-scale decoder-driver MOSFET, and delivers a cell current of 20 μA/bit and 50 MHz operation at 1.5V. The combination of a low programming current of 1 μA/bit and elimination of the need for negative bias in erasing leads to a small voltage circuit. So, with a 0.18-μm process, the size of a 512 kB flash memory module is reduced to 5.4mm^2.

1. Introduction

Strong demand for microcontrollers that include embedded non-volatile (most of flash) memory has been generated by the ease of debugging and modifying the system programs of such devices. To embed a suitably large memory in such a controller, we need to apply device-scaling techniques. Such techniques are also important because a small flash-memory module leads to lower production costs. Since portable devices are a major market for microcontrollers, we need to achieve low-voltage operation. Moreover, we still need to maintain high reading speed. We have advanced in both directions by developing a new split-gate-type MNOS memory cell where the controlling MOS transistor has an unprecedented thin gate-oxide.

2. Cell Structure and Fabrication Process

The memory cell has a split-gate-type structure in which the gate electrode of the MNOS memory (MG) is independent from that of the control gate (CG). The layout and cross-section of the cell, fabricated with a 0.18-μm process, are shown in figure 1. The cell size is 0.54 μm^2. Programming is by source-side hot-electron injection, and erasing is by tunneling to the MG while a positive bias is applied to the MG. This combination reduces the area of voltage-source circuit, since both operations only require positive bias. To improve the cell-reading current, the gate oxide of the CG is formed with the same thickness as that of the core MOS transistors of the peripheral low-voltage circuits. This also lets us use smaller devices in the decoder circuits that drive the CG. So, the total size of a flash memory module with capacity of 512 kB is reduced to 5.4 mm^2 [1].

The memory-cell fabrication process is shown in figure 2. The MNOS is the first active device to be formed on the substrate. The bottom 4 nm-thick oxide layer is formed by thermal oxidation. Silicon nitride and non-doped polysilicon are deposited, in that order. The non-doped polysilicon is given a dose of P after deposition, to turn it into n-type MG polysilicon. These films are etched anisotropically to form the individual devices. Oxide spacer is formed on the side-wall of each MNOS device. This is a key structure in forming of a thin gate oxide layer for the adjacent CG. Polysilicon is deposited for both the CG and the gate electrode of the MOS transistors of the peripheral circuit.

3. Device Characteristics

The cell-current vs. MNOS-gate voltage characteristics for cells in the programming and erasing states are shown in figure 3. The read current of 20 μA required in the erased state with both CG and MG biased at 1.5V enables operation of the flash memory module at 50MHz.

Figure 4 shows the programming/erasing characteristics, with the values for a MONOS device given for comparison. Programming current is 1 μA/bit, and programming takes less than 10 μs. Erasing of the MNOS device is completed within 10 ms, which is shorter than the time for the MONOS device, even though the total physical thickness of the ON film is almost the same as that of the ONO film. The top oxide formed between the MG and nitride prevents fast tunneling of electrons to the MG from nitride.

The verified endurance characteristic is shown in figure 5. Both programming time and erasing time remain stable through 1,000 cycles of programming/erasing.

A sample retention characteristic is shown in figure 6. The threshold voltage of programming state remained above 2 V after 10 years at 125 ℃ with 0V on the MG in the case where the bottom oxide is 4-nm-thick. Tunneling to the MG as the erasure mechanism allows us use to a thicker bottom-oxide layer than that of a conventional MONOS device [2], and this prevents the discharge of electrons to the channel. MNOS is consistent with fast erasing and good data retention (figure 7).

4. Conclusions

We have presented a new split-gate-type MNOS memory cell with a thin gate-oxide layer for the CG. This

thin gate oxide obtains an operating frequency of 50 MHz at 1.5V. Reduction of the areas of voltage-source circuits and decoder drivers brought us a small flash-memory module, with 512 kB in only 5.4 mm^2, with 0.18-μm process.

Acknowledgements

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References

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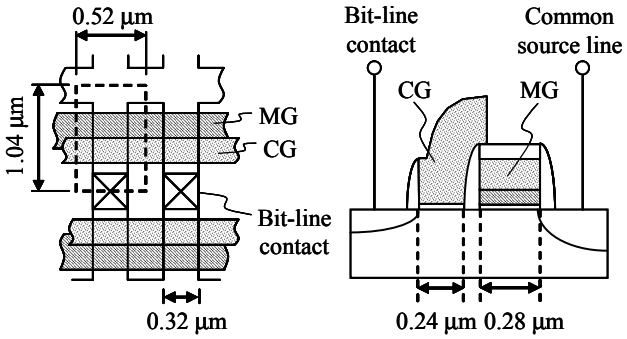

Fig.1 Cell layout and cross section

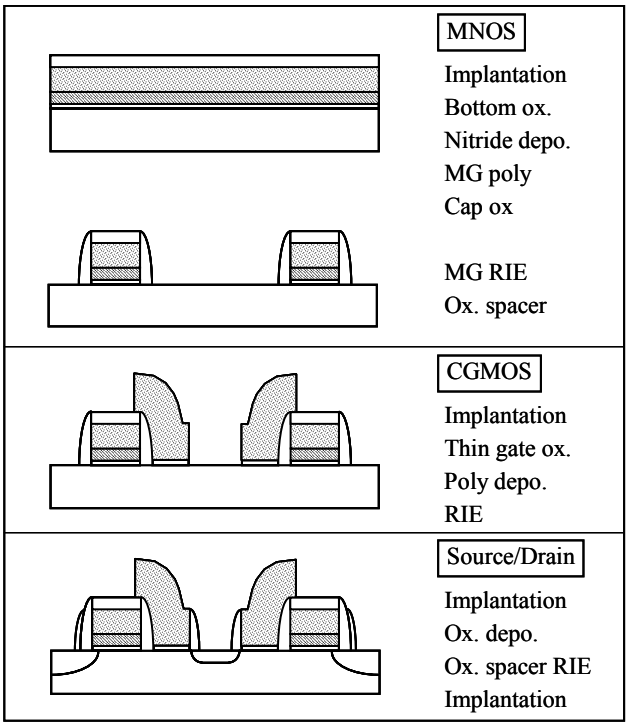

Fig. 2 Cell process sequence

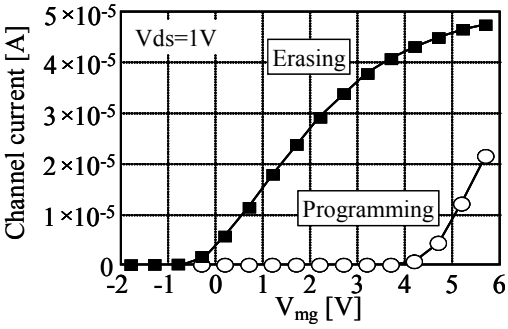

Fig. 3 Memory cell current

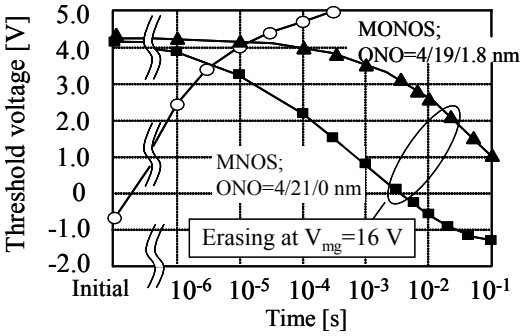

Fig. 4 P/E characteristics

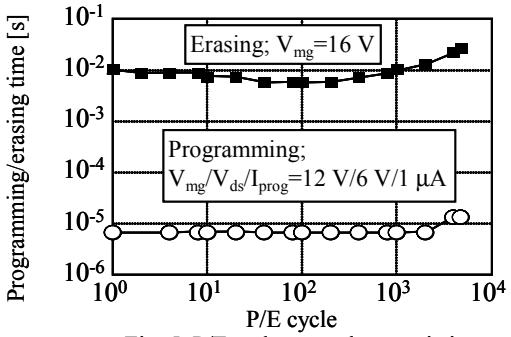

Fig. 5 P/E endurance characteristics

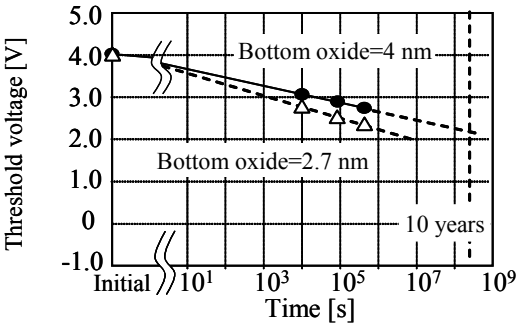

Fig. 6 Data retention characteristics

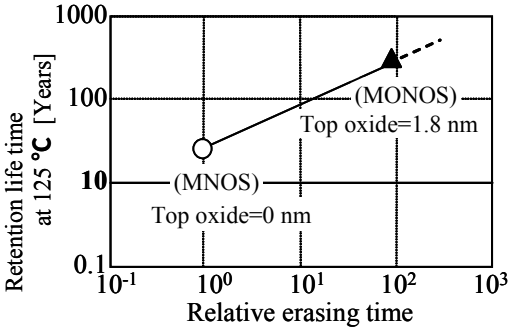

Fig. 7 Trade-off between erasing time and retention life time