70 nm SONOS Nonvolatile Memory Devices using FN Programming and Hot Hole Erase Method

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1. INTRODUCTION

The Si floating gate structure is widely used in Flash Electrically Erasable Programmable Read Only Memory (EEPROM). The floating gate type EEPROMs employ tunneling oxides thicker than 7 nm, which are required to guarantee retention characteristics, and need high voltage operation due to programming/erase electric fields over 6 MV/cm [1]. The International Technology Roadmap for Semiconductors (ITRS) also indicates that it would be a difficult challenge, beyond the year 2005, for floating gate type EEPROM to achieve both of reliability and low voltage operation [2]. However, advancements in ultra-thin gate dielectrics have opened a path to both low voltage operation and long retention characteristics based on Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) technology. In addition, the continued scaling of SONOS devices offer improved performance with a small cell size for high-density semiconductor memory applications [1].

In this paper, we present the fabrication of scaled-down SONOS memory cell with 70 nm gate length on the ultra-thin Oxide-Nitride-Oxide (2.3/12/4.5 nm) film for vertical scaling, and the characteristics of the fabricated devices. Our focus is specially on an improved erase characteristics by 2-side hot hole erase and low voltage operation.

2. FABRICATION

We fabricated 70 nm gate length and 30 nm channel width SONOS memory devices on silicon-on-insulator (SOI) substrates using conventional CMOS process technology. The channel was defined by the sidewall patterning method. The channel implantation was performed with BF_2^+ ions and 2.3-nm-thick tunneling oxide was grown at 900 °C. Subsequently, a Si_3N_4 film of 12 nm and the blocking oxide layer of 4.5 nm was deposited by Low Pressure Chemical Vapor Deposition (LPCVD). After the poly-silicon gate patterning using the sidewall patterning method, n^+ source/drain extension region was formed with low energy As_2^+ ion implantation. Finally, deep source/drain regions were formed by implanting As^+ ions and the rapid thermal annealing was carried out to activate. Fig. 1 shows the cross-sections of the device across the channel.

3. RESULTS AND DISCUSSION

Fig.2 shows the transfer characteristics of the fabricated devices. The subthreshold swing is about 90 mV/dec, on 70 nm nMOSFETs with 2.3 nm thermal oxide, 12 nm nitride, and 4.5 nm LPCVD oxide. Tthey also illustrate that its shallow S/D extension suppresses drain induced barrier lowering (DIBL), which is less than 30 mV.

Fig. 3 shows programming speed characteristics by the Fowler-Nordheim (F-N) tunneling current. As the programm-ing voltage increases, the programming time improves. If we take the program/erase threshold voltage window as 2 V, the program time is about 1 ms at 8 V program voltage, and this programming time is short enough for the use of semiconductor memories as massive data storage [3]. In the case of erase time characteristics by F-N tunneling method, the erase time is about 100 ms for the same threshold voltage window at –8 V erase voltage, as shown in Fig. 4. The erase time is somewhat slow, and it is due to the electron injection through top oxide from gate. To solve this problem, we used hot hole erase method as bias conditions [4]. Fig. 5 and Fig. 6 shows erased characteristics of SONOS Cells as a function of erasing time for various source and gate bias, respectively, by 1-side hot hole erase method. The erase time by 1-side hot hole erase method is not faster enough for practical applications. Fig. 7 shows the erased threshold voltage vs. time for several bias conditions of 2-side hot hole injection. The erase time is about 1ms with 2.5V memory window and improved by a factor of 2 compared with previous bias conditions. These improved results can be explained by erasing the whole electrons charged in silicon nitride using 2-side hot hole erase method [4].

Fig.8 shows the endurance characteristics after various number of erase and write cycles. The memory window was almost constant after 100,000cycles by FN programming and 2-side hot hole erase. The retention characteristics are shown in fig. 9. The threshold voltage after 10^6-retention was predicted to 0.75V by extrapolation.

4. CONCLUSION

We fabricated 70nm SONOS memory cells with an ultra-thin ONO film on an SOI wafer and characterized using FN programming and 2-side hot hole erase injection. The erase characteristics of our devices was improved using 2-side hot hole erase method. In addition, good endurance and retention characteristics were obtained from this work.

5. REFERENCE

[1] M.H. White et al, IEEE Circuits and Devices Magazine, Vol. 16, Issue 4, pp. 22 –31, July 2000
[2] The International Technology Roadmap for Semiconductors (ITRS), Table 38a, 38b, 2001
[3] Margaret L. French et al, IEEE Trans. on component, packing and manufacturing technology – part A, Vol. 17, No. 3, pp. 390-397, September 1994
[4] E.J.Prinz et al, Non-volatile Semiconductor Memory Work shop, pp.56, 2003
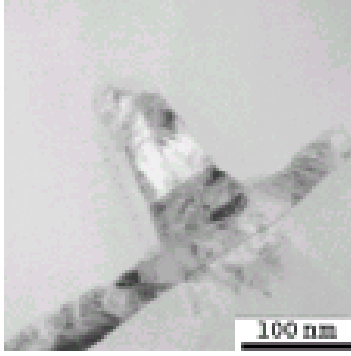
6. ACKNOWLEDGEMENT

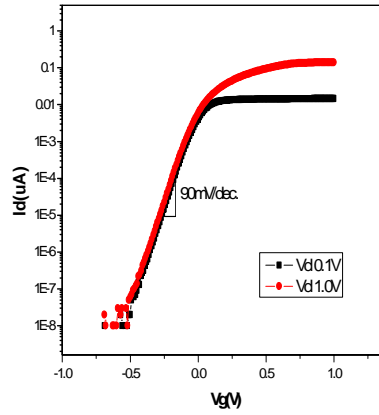Fig. 1 70-nm long poly-silicon gate TEM image.

Fig. 2 Subthreshold swing and DIBL characteristics. Subthreshold swing is about 90 mV/dec. and DIBL value is less than 30 mV.
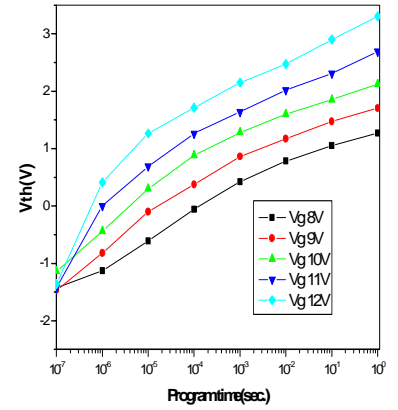

Fig. 3 F-N programming time characteristics. The programming time is about 1 ms at 8 V control gate voltage, if we take 2 V programming V_{th} window.
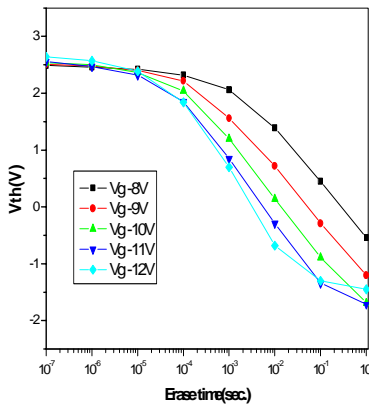

Fig. 4 F-N erase characteristics. If we take erase V_{th} window as 2 V, the erase time is about 100 ms at -8 V control gate voltage.
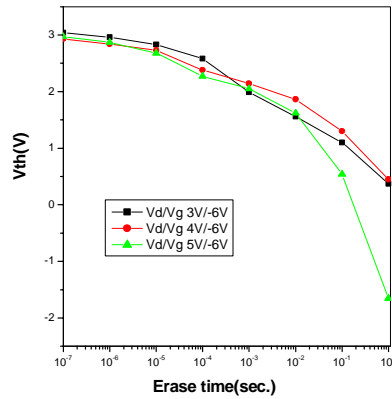

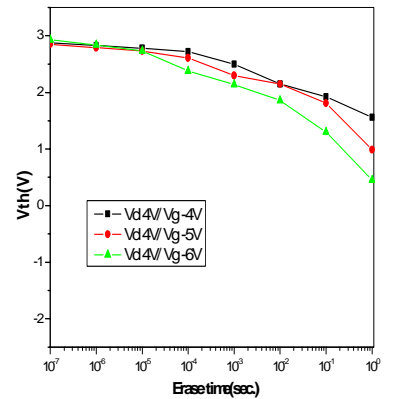Fig. 5 1-side hot hole erase characteristics when increasing drain voltage.

Fig. 6 1-side hot hole erase characteristics when increasing gate voltage.
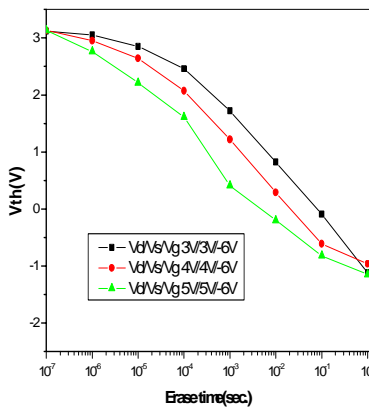

Fig. 7 2-side hot hole erase characteristics. When Control gate voltage is –6 V and drain/source voltage is 5 V, Erase time is reduced to below 1 ms.
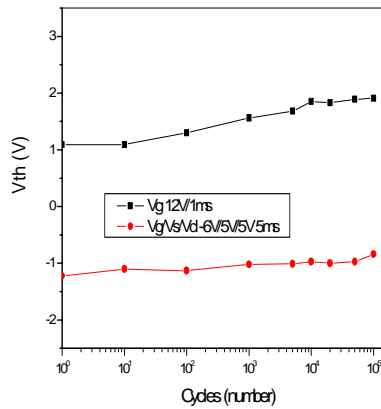

Fig. 8 Endurance characteristics. These characteristics guarantee more than 100,000 cycles using FN progrmming and 2-sided hot hole erase method.
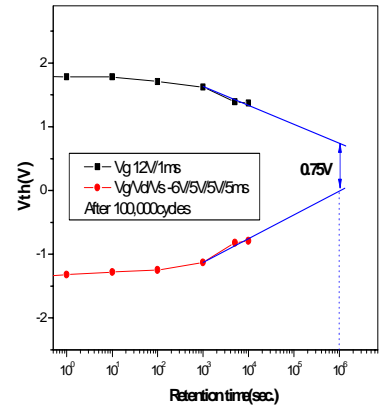

Fig. 9 Retention characteristics. These characteristics guarantee 0.75V threshold voltage window for more than 10^6 s at 85 °C.