Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 224-225

B-6-1

Hot Carrier Injection/Fowler Nordheim Erase Silicon Nanocrystal Memory Cell

R. A. Rao, R. F. Steimle, M. Sadd, C. Swift, R. Muralidhar, B. Hradsky, S. Straub, E. Prinz, J. Yater, and B. E. White Jr.
Motorola SPS, Austin, TX 78721, USA. (Tel: 512-933-7099, FAX: 512-933-3249, rajesh.rao@motorola.com)

Introduction

Scaling of floating gate (FG) non-volatile memory cell has been limited to bottom oxide thicknesses in the range 90-110Å primarily because of the vulnerability to charge loss from the conducting floating gate through isolated defects in the tunnel oxide, primarily after write/erase cycling. SONOS [1,2] and silicon nanocrystal based memory cells[3,4] that store charge in discrete and isolated centers inside a gate dielectric have been proposed to scale tunnel oxide. For NVM applications, read disturb and data retention criteria limit bottom oxide thickness to the range of 50–70Å to suppress defect site mediated charge exchange with the channel. In this paper we demonstrate superior Fowler/Nordheim tunneling characteristics of nanocrystal memory compared to SONOS that permit conventional HCI/FN operation and show that this memory cell can potentially provide a scaling path to floating gate technology by reducing the total gate stack thickness. In addition, we show that the deep silicon nanocrystal traps permit excellent charge isolation in the FG for potential 2 bit per cell operation. All devices shown in this paper have been fabricated using 0.13µm CMOS technology. The silicon nanocrystals (Figure 1) were deposited at required densities using optimized CVD processes and were in the range $5x10^{11}$ cm^{-2} to $1.1x10^{12}$ cm^{-2} as measured on active areas. Memory cells were fabricated with different areal coverages of silicon nanocrystals ranging from 15% to 50%. While, the control oxide in SONOS was obtained by oxidizing back a thicker nitride layer, in the case of the nanocrystal memory cell the control oxide was a high temperature CVD oxide. In this paper, all Si nanocrystal memory cell data have been obtained from 0.13µm channel length devices.

Fowler-Nordheim Erase

The typical tunnel erase behavior of SONOS is shown in Figure 2. As the erase bias is increased, it proceeds faster but saturates at a higher threshold voltage. This erase saturation arises from a balance between the current through the bottom oxide and competing electron injection from the gate. In SONOS, the erase current through the bottom oxide is less responsive to the field, but attenuates more rapidly with increasing tunnel oxide thickness than the competing back injected current through the top oxide. As a result, the saturated threshold voltage at which the competing currents balance each other increases with both erase bias and tunnel oxide thickness, so that it is not practical to erase a SONOS bit-cell with a tunnel oxide thicknesses greater than 5nm with tunneling. Hence, hole injection [2] has to be used and the reliability of tunnel oxides has to be established. In contrast, silicon nanocrystal memories show no such bias dependence of erase saturation. As Figure 3 shows, increasing the tunnel erase bias increases the speed of erase and saturates at about the same threshold voltage. Because the field dependence of the electron current from the nanocrystals to the substrate is similar to the field dependence of the competing current from the gate, erase saturates at the same threshold voltage nearly independent of bias.

Programming of silicon nanocrystal memory by FN electron injection from the channel is dependent on the geometrical characteristics of the silicon nanocrystals. Referring to the band diagram in Figure 4, when electrons are injected into the nanocrystal from the substrate, the control oxide field along the nanocrystal becomes greater than the tunnel oxide field (high local charge density) and this facilitates removal of electrons from the nanocrystal to the gate, thus preventing programming for memory cells with low areal coverage of nanocrystals (Fig 5 top image). When the nanocrystal density is very large (see bottom Figure 5) or we have a 3-dimensional network [4], electrons can rapidly tunnel from one nanocrystal to another making the gate resemble a continuous floating gate. Since, the local large control oxide field is absent in this case and electrons can be captured by larger cross-section, limited programming by FN is possible. Ultimately, saturation sets in when currents from the channel to the nanocrystal and from the nanocrystal to the poly-Si gate are in balance. Figure 6(a) and (b) shows the FN programming curves for devices with small and large areal coverage respectively and it is evident that devices using a single layer of well isolated silicon nanocrystals are not programmed. At 8V, both devices are in the direct tunneling regime in the 38Å tunnel oxide and FN tunneling in 100Å control oxide with the former being faster of the two. Hence, limited charge injection into the nanocrystals is possible.

Hot Carrier Programming/Fowler-Nordheim Erase

Effective hot carrier programming of a silicon nanocrystal bit cell can be attained for different gate and drain biasing conditions. Figure 7(a) and (b) show the program curves for different drain biases and gate biases respectively. It is evident that a 2V threshold voltage shift can be obtained with sub 10 microsecond programming time. A typical erase curve is shown for the same bit and indicates that 100 milli-second block erase can be achieved. Figure 8 shows the program and erase cycling endurance of the cell with a 50Å tunnel oxide and 100 Å control oxide. The program and erase threshold voltage drifts up possibly due to charge trapping in the control oxide. Unlike a floating gate device that captures all hot electrons injected towards the gate, the nanocrystal FG has less capture cross section and hence electron trapping in control oxide must be minimized by optimizing control dielectric. Figure 9 shows excellent data retention at 150°C as well as excellent read disturb characteristics after 1000 program and erase cycles.

Local Storage and 2 bit per cell operation

The isolated nature of charge storage centers and the energy well (3.1eV to silicon dioxide) makes the nanocrystal memory cell a good candidate for local storage. Figure 10 shows the asymmetric threshold voltages obtained by forward and reverse reading operations [2] in a 0.13µm channel length device with nanocrystal area coverage of 20%. It is seen that at such low area coverage, excellent local storage and data retention is observed. At higher area fractions, lateral tunneling transport prevents local storage.[5]

Conclusions

This paper shows that silicon nanocrystal memory cell can offer a scaling path to floating gate flash by permitting tunnel oxide thickness reduction to about 50A using conventional hot carrier injection programming and Fowler-Nordheim erasure. This arises from excellent charge isolation as well as desirable FN erasure characteristics that are absent in SONOS with thicker bottom oxides. Additionally, the ability to store charge locally at the edges of short gates (0.13µm) has been demonstrated that will enable 2 bit per cell operation

References

[1] M. H. White et al, in "Nonvolatile Semiconductor Memory Technology", W. D. Brown and J. E. Brewer, edt IEEE press, 1998.
[2] Boaz Eitan, Intl. Conf. Solid State Dev. Matls, Japan, 1999.
[3] T. Tiwari, et al. IEDM Technical Digest, 20.4.1 ,1995
[4] J. De Blauwe et al., International Electron Devices Meeting, 2000
[5] B. Hradsky et al, IEEE Non-Volatile Memory Workshop 2003

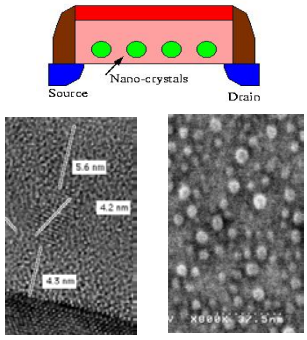

Fig. 1. Schematic of nanocrystal memory (top), cross sectional TEM (left) and plan-view SEM images (right) from nanocrystal memory bit cells.

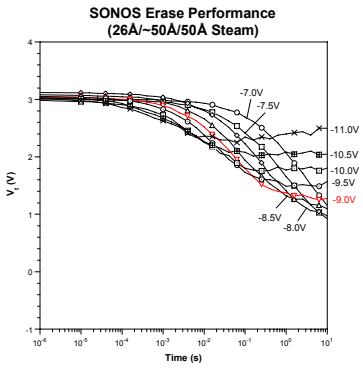

Fig 2. Typical FN erase of a 26A tunnel oxide, 50A nitride and 50A control oxide SONOS bit showing bias dependent erase saturation.

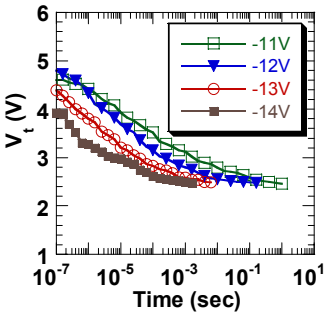

Fig. 3. FN erase at various gate bias for a nanocrystal memory device with 45A tunnel oxide and 100A control oxide showing bias independent erase saturation.

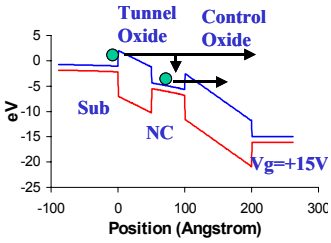

Fig. 4. Energy band diagram of nanocrystal memory under positive gate bias of 15V showing FN tunneling across bottom and top oxide.

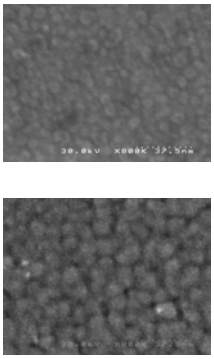

Fig. 5. SEM images of nanocrystals with low areal coverage of 25% (top) and high areal coverage of ~ 50% (bottom) deposited on tunnel oxide.

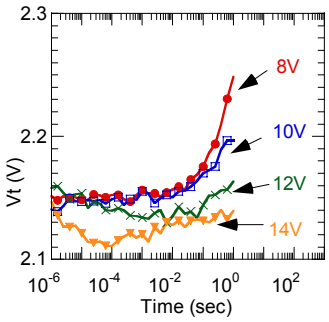

Fig. 6(a). Programming curves at various gate biases for a bit cell with 38A tunnel oxide and 100A control oxide with 25% nanocrystal coverage.

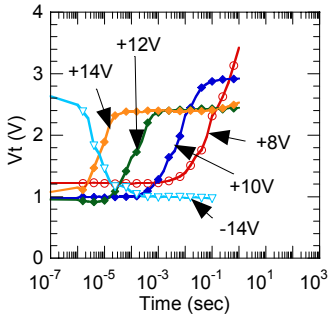

Fig. 6(b). Programming curves at various gate biases for a bit cell with 38A tunnel oxide and 100A control oxide with 50% nanocrystal coverage.

.

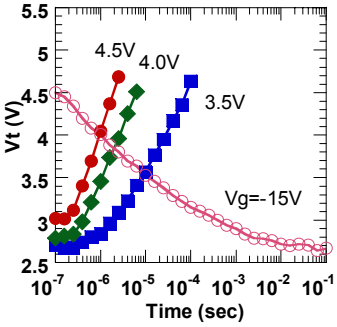

Fig. 7(a). Influence of drain bias on HCI programming speed at Vg=10V for a bit cell with 50A tunnel oxide and 100A control oxide.

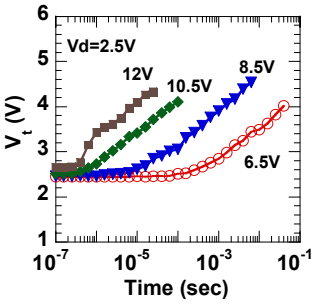

Fig. 7(b). Influence of gate bias on HCI programming speed at Vd=2.5V for a bit cell with 50A tunnel oxide and 100A control oxide.

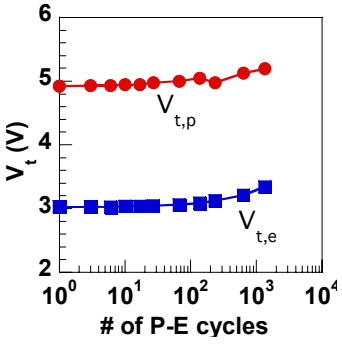

Fig. 8 HCI program (Vg=9V, Vd=4.5V; 1.5µsec) and FN Erase (Vg=-15V; 0.1sec) cycling endurance behavior of a memory cell with 50A tunnel oxide and 100A control oxide

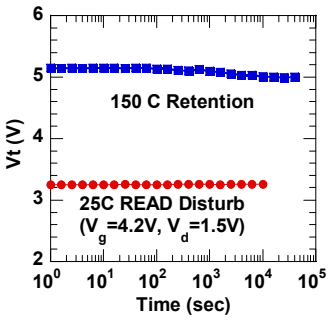

Fig 9. 150C Data retention of high Vt state and 25C Read disturb for a 50A tunnel oxide nanocrystal memory cell after 1000 cycles of program and erase.

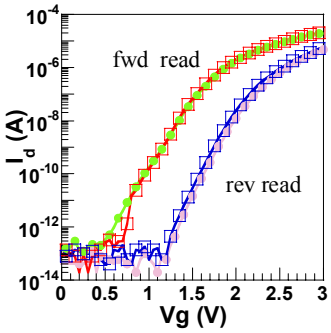

Fig. 10 Id-Vg curves at t=0 (solid circles) and t=65hours (open squares) showing local storage data retention at 150C after localized CHE programming for 55A tunnel oxide with ~ 20% areal coverage of nanocrystals.