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A New Investigation on Erase V_T Variation of NOR Flash fabricated with 90 nm Technology

T.Y. Kim, W.H. Lee, J.I. Han, S.E. Lee, H.G. Lee, S.Y. Kim, J.H. Park, S.W. Park, J.H. Choi, M.K. Cho, Y.H. Song, and Kinam Kim

Advanced Technology Development Team, Semiconductor R&D Center, Memory Business, Samsung Electronics Co., Ltd.
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyungki-Do, Korea, 449-711
Phone: +82-31-209-2660 E-mail: t-yong.kim@samsung.com

1. Introduction

As the NOR flash enters into sub-100 nm technology node, there appeared to be several issues to seriously limit NOR flash scaling. Among those restrictions, the large fluctuation of V_T in erase states seems to be one of the most difficult tasks to solve, especially for flash memories with multi-level cells (MLC). Many efforts have been devoted to tightening the V_T distribution by the process optimization. However, as the design rule is scaled down to nm-scale regime, some unexpected factors, for instance, the parasitic capacitance coupling between adjacent floating gates (FGs) in NAND[1], could appear to make the V_T distribution worse. Among these, in this paper, we report for the first time the effect of a parasitic capacitance originated from the misalignment of the bit-line (B/L) contact on the V_T shift of the erased state.

2. Experiments

The layout of cell array is shown in Fig. 1 and cell has a channel width/length of 90/150 nm. The space for BL contact between FGs is 260 nm where the contact size is 100 nm. The NOR flash cells are fabricated with a 90 nm technology with self-aligned shallow trench (SA-STI) and self-aligned source (SAS) structure. The key features of 90 nm NOR Flash technology was reported elsewhere [2].

3. Results and Discussions

In Fig. 2, we have calculated the erased V_T with the key process parameters that could give rises to the V_T distribution. The key process parameters are illustrated with their notations. It should be noted that the effect of the misalignment of B/L contact on the erased V_T has been considered to be negligible down to 120 nm NOR Flash technology compared to other key parameters such as tunnel oxide thickness, active width, and ONO thickness, etc. However that is no longer true in nm-technology. As shown in Fig. 3, considering the actual range of the process parameters, the variation in erase V_T could be more sensitive to S_{mc} (B/L contact space) than the others in 90-nm technology. In other words, the smaller room for B/L contact space (S_{mc}) as the design rule is scaled down, the more difficult to control the misalignment of B/L contact, so that it could be one of the most difficult issues to be eliminated in nm technology.

Fig. 4 shows that the B/L contact is misaligned toward the odd cell in the SEM image. When it happens, the coupling capacitance between FG and B/L due to the misalignment of B/L contact is not same in both of odd and even cells. The odd cell has a larger capacitance (C_{CNT}) than the even cell since the dielectric layer thickness is decreased. As a result, the coupling ratio is to be affected by an parasitic capacitance induced by the misalignment of B/L contact. When the C_{CNT} is considered as an additional term, the total capacitance of FG (C_T) is given by

$$C_T = C_{ONO} + C_S + C_D + C_{CH} + C_{CNT}\,, \qquad (1)$$

where their notations are depicted in Fig. 4.

Fig. 5 shows the erase V_T distribution of perfectly aligned (a) and 22 nm-misaligned cells (b). In the perfectly aligned cells, the erase V_T distribution for the odd and even word lines (W/Ls) is not different from each other. However, in the case of 22-nm misalignment that corresponds to 31% variation of S_{mc}, the distribution of odd W/L is located at as much as 0.5V more than that of even W/L. This variation depending on even and odd W/Ls can be clearly explained by considering the parasitic capacitance due to the misalignment of B/L contact. As the C_{CNT} is larger in odd cells than even cells, the odd W/L has a larger total capacitance, leading to a smaller coupling ratio.

We have estimated the contribution of S_{mc} to the variation of erase V_T for the several generations in Fig. 6. In 100-nm space of MC to gate corresponding to 120-nm technology, the contribution of S_{mc} is not crucial. However, for 90-nm technology corresponding to the 80-nm space for MC to gate, the variation of V_T begins to be dramatically sensitive to S_{mc}. Thus, it is essential to precisely control the misalignment of B/L contact in nm technology.

Fig. 7 shows the result of the erased V_T shift between odd and even W/Ls for the misalignment. The simulated data by eqn. (1) are agreed with the measured ones, which means that the parasitic capacitance due to the misalignment of B/L contact has an important role in V_T variation. Therefore, in NOR flash, the process free from the misalignment of B/L contact, for example, the Self-Aligned Contact (SAC) process, should be considered in nm-scaled technology.

4. Conclusions

We have investigated an additional factor influencing the erase V_T distribution in 90-nm technology. The misalignment of B/L contact is no longer negligible due to the parasitic capacitance between FG and B/L contact. When the misalignment of B/L contact is increased, the curve of the erase V_T distribution is splitted to two curves, which could result in the poor distribution of the erase V_T.

References

[1] J.D.Lee et al., IEEE Electron Device Letters, p.264, (2002).
[2] Y.H.Song et al., Dig. of VLSI Symp., to be puplished (2003).

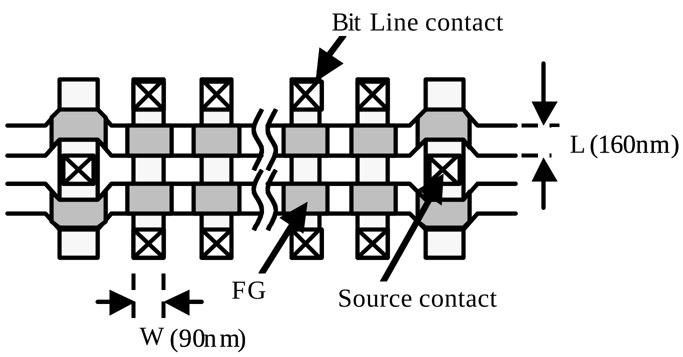

Fig. 1 Schematic layout of NOR flash cell array. W and L are the active width (90nm) and channel length (150nm), respectively. The size of B/L contact and space are 100nm and 260nm.

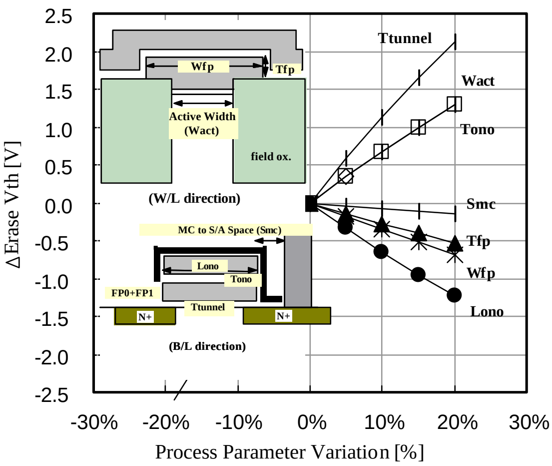

Fig. 2 The simulated results for erased V_T sensitivity with respect to the key process parameters which are the thickness of tunnel oxide (T_{tunnel}), the width of channel (W_{act}), the thickness of ONO (T_{ono}), the space of B/L contact to the gate (S_{mc}), the thickness of floating gate (T_{fp}), the width of floating gate (W_{fp}), and the length of ONO (L_{ono}).

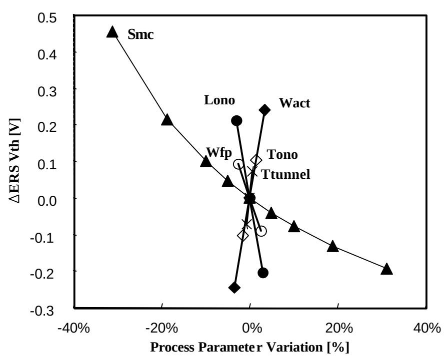

Fig. 3 The V_T variations with the process parameters, where the S_{mc} parameter seems to be the most important factor in 90-nm technology.

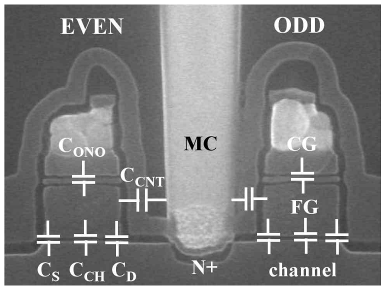

Fig. 4 SEM image of misaligned cell, where a bitline contact is shifted to the odd cell, touching the SiN layer. C_{ONO} = capacitance between FG and control gate, C_S = capacitance between FG and source, C_{CH} = capacitance between FG and channel, C_D = capacitance between FG and drain, and C_{CNT} = capacitance between FG and B/L contact.

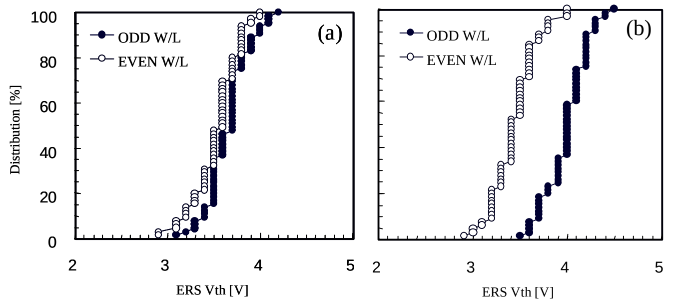

Fig. 5 The erase V_T distribution for (a) perfectly aligned and (b) 22nm-misaligned cells. For the case (b), the distribution curve is clearly splitted into two curves.

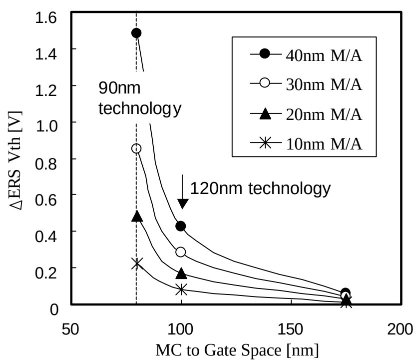

Fig. 6 The simulated data of the contribution of S_{mc} to the variation of erase V_T. In the 90-nm technology corresponding to 80-nm space of MC to gate, the dramatic change is observed.

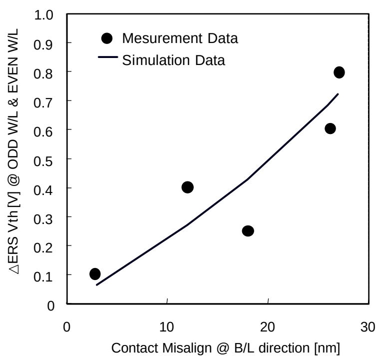

Fig. 7 The difference of erase V_T between the odd and even W/L is plotted vs. the amount of the misalignment.