Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 228-229

**B-6-3L**

# Vt drift of Cycled Two-Bit *micro*FLASH® Cells.

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## 1. Introduction

Compared with conventional SONOS type Flash memory, where charge is stored uniformly in the Nitride layer, *micro*Flash® [1)] memory features localized charge trapping at the edges of memory transistor channels. Channel hot electrons (CHE) are used for programming and band-to-band (BBT) hot hole injection is used for erase Reverse read scheme and local charge allow two-bits per cell operation [1]. Both electrons and holes are simultaneously trapped in ONO in the erased state. The aim of this paper is to investigate the physical mechanisms that limit Vt stability of *micro*FLASH. We focus on two models, one attributing the observed Vt shifts in programmed and erased states to lateral migration of charges trapped in the Nitride of ONO while the other model accounts for the bottom oxide degradation.

## 2. Two Models of Vt drift

Programmed-only *micro*Flash Vt decreases less than 100mV after standard (250C/24h) retention bakes. Corresponding activation energy is 1.7-1.8eV [2]. Additional "fast" Vt loss with low activation energy (~0.3eV) is registered after cycling and bake. It has a value of 250-500 mV after 10k-100k cycles. Vt of the erased state of the cycled cell increases with time. The increase is also limited and weakly temperature activated.

The first degradation model attributes Vt shifts to lateral movement of trapped electrons and holes. The centroids of the electron and hole charges are misaligned due to different injection points of CHE and BBT holes[3]. Holes were shown to be more mobile. Their movement can change the amount of charge over the channel region and as a result the Vt and read current are changed.

The results of an experiments that proves lateral hole migration are shown in Fig.1. A fresh cell was erased for a long time by injecting large positive charge into ONO. The cell was then baked at 250C for a few hours. A BBT monitor (voltage resulting in given GIDL current increase at Vd=2V) was used to sense the charge trapped over the drain of the memory transistor. The threshold voltage that is sensitive to the charge over the channel region was measured in parallel. After long erase, positive charge was trapped in ONO in the channel region and over the drain. This follows from the reduction of Vt and the increase of BBT monitor. After the bake, positive charge moved laterally inside the channel and Vt of the cell became lower. Positive charge density over the drain region decreased causing the BBT monitor to shift back to its initial value.

Both positive and negative gate stress after 100 cycles result in a much less Vt drift of the erased state (Fig.2). This fact can be explained by F-N injection of electrons into the region with trapped holes (Fig.3). Bakes with low voltages (1-5V) at the gates gave similar results and further confirmed the two-charge model (Table.1). The 100 times cycled cell shows ~ 300mV Vt drift of the erased state. Bake with voltage at gate almost removed the Vt increase.

In the second model the charge retention loss is explained by bottom oxide degradation. Trap generation in the bottom oxide is a common issue in the floating gate Flash memories. This mechanism was also discussed for products similar to *micro*FLASH in [4]. Our experiments also show signs of bottom oxide degradation but after much large numbers of cycles than 1k mentioned in [4]. Examples of results confirming bottom oxide degradation after cycling are shown in Fig.4 and Fig.5. Accelerating gate stress was applied to fresh and 10k cycled cells. One can see that gate stress influences the Vt of cycled cells only. Negative Vg stress reduces Vt and positive Vg stress increases Vt of the programmed cell. Basically, SONOS is a symmetrical system where positive or negative gate stresses must cause the same Vt shift if one considers only holes trapped in Nitride. Additional experiments were performed to study the traps in bottom oxide. In one of the experiments the cycled cell (10k) was programmed and then baked at moderate temperature 150C (instead of 250C) for a long time. Low temperature was selected in order not to anneal the traps in bottom oxide. A typical "fast" Vt loss was observed after the 150C bake. After that the gate stress was applied. The Vt increase (absent for fresh cells) was nevertheless observed. This is not consistent with the model of lateral migration. The discussed peculiarities of Vt shifts prove the additional influence of bottom oxide traps created during cycling.

## 3. Conclusion

Both lateral hole migration in Silicon Nitride and traps in bottom oxide after cycling are responsible for Vt shifts in *micro*FLASH SONOS cells. The influence of bottom oxide degradation becomes significant for large numbers of cycles.
The corresponding shifts are taken into account when defining the program/erase margins of 10k-100k *micro*FLASH products.

[1)] *micro*Flash is a registered trade mark of Tower Semiconductor Ltd.

## References


[1] B.Eitan, *US Patent* 5,768,192, June 16, 1998.
[2] Y. Roizin, et al, IEEE NVSM Workshop (2001, Monterey, CA), p.128.
[3] E.Lusky, et.al, IEEE ED Lett, **23**, (2002) p.556.
[4] W.J. Tsai, et al, IEDM Tech.Dig. (2001), p.719.


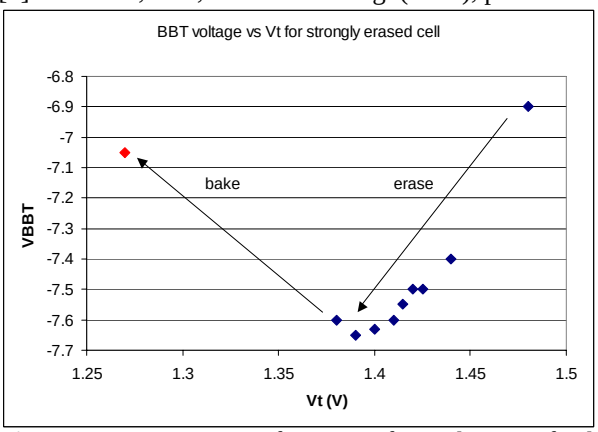


**Fig.1** BBT monitor as a function of Vt, showing fresh cell long erase followed by 250C bake

**Vt increase in erased state after cycling and gate stress.**

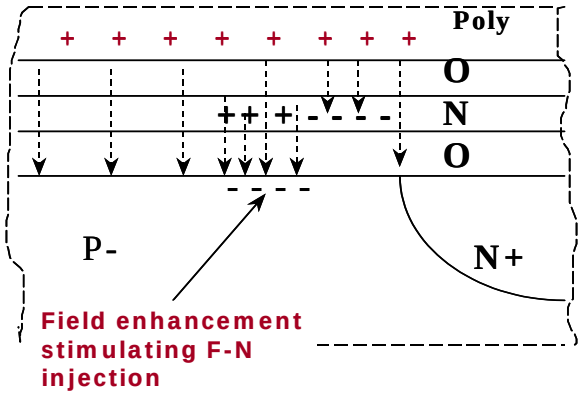


**Fig. 3** Gate stress is superimposed over the vertical field of trapped holes and results to F-N injection from electrodes.

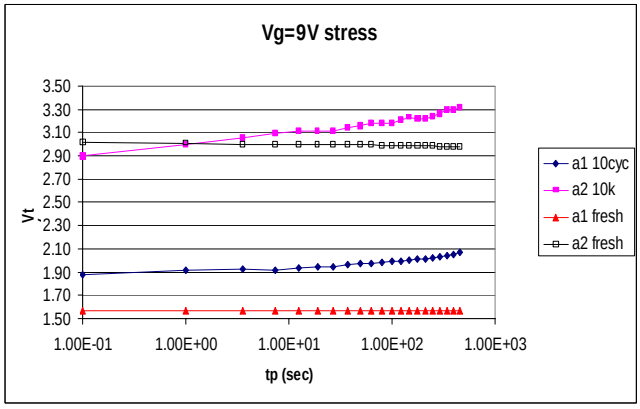


**Fig. 5** Vg stress accelerates Vt shift after 10k cycling. Positive Vg stress increased Vt of programmed and erased cell (tp is the time of stress; a1/a2-opposite direction of Vt measurement)

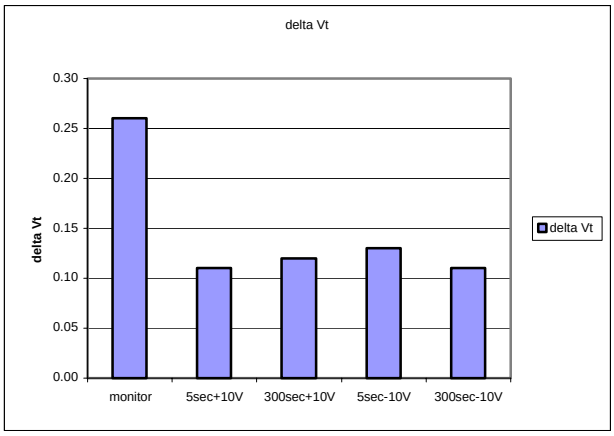


**Fig. 2.** Both negative and positive stresses of cycled cell in erased state result in Vt shift (stress was applied after cycling in the programmed state; after erase Vt drift was measured) .

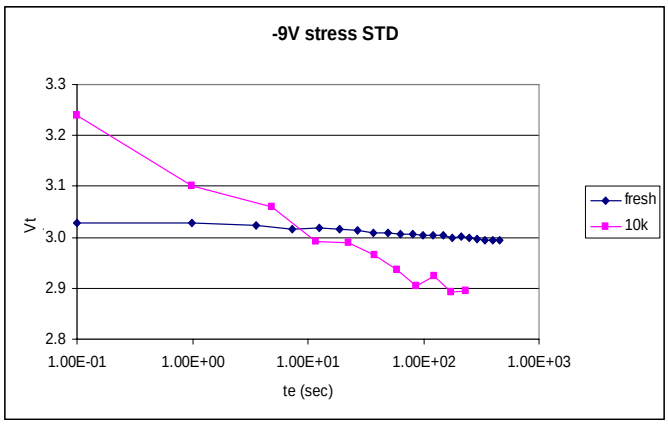


**Fig. 4** Vg stress accelerates Vt shift after 10k cycling. Vt of programmed cell decreases (te is the time of stress)

**Table 1**

| Vg | Vt shift | comments |
|---|---|---|
| 0V | 300mV | No bake and No Vg stress |
| -5V | 0mV | After 200C 1 hour bake with Vg= –5V |
| -3V | 50mV | After 200C 1 hour bake with Vg= –3V |
| -1V | 50mV | After 200C 1 hour bake with Vg= –1V |
| 3V | 0mV | After 200C 1 hour bake with Vg= 3V |
| 5V | 0mV | After 200C 1 hour bake with Vg= 5V |

Vt drifts (one week; 25C) of 100 times cycled cells after the bake with different voltages at the gate.