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Low Tinv (≤ 1.8 nm) Metal-Gated MOSFETs on SiO_2 Based Gate Dielectrics for High Performance Logic Applications

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Abstract

We present results on mid-gap metal gated MOSFETs using $CoSi_2$ & W with Si oxide & oxynitride gate dielectrics. For $CoSi_2$ gates, we demonstrate a simple integration scheme using silicidation of the polysilicon (poly) gate with low nFET Tinv~1.7nm. For the W gate stack, we use a replacement gate process resulting in a pFET Tinv~1.8 nm. W pFET mobility is comparable to poly, while nFET peak mobility is degraded.

1. Introduction

Beyond the 90nm node, the integration of new materials, such as high-k dielectrics and metal gates would be paramount for advanced CMOS applications. Introducing metal gates first can obviate the problem of poly depletion in inversion, eliminate boron penetration & circumvent problems associated with metal oxide high-k dielectrics. A dual metal gate solution would be ideal, but difficult to identify & implement into devices. Instead, a single midgap metal could be used with the Vt adjusted by suitable implants. In the present work, we realize this by using two integration schemes, silicidation of gate poly ($CoSi_2$) & a replacement gate process (W), at gate dimensions ranging from 0.1 to 10 μm. In both cases, the gate leakage current for the same Tinv was reduced by an order of magnitude relative to poly/oxynitride and Tinv ≤ 1.8 nm achieved with conventional dielectrics.

2. Process Integration

Cobalt Silicide Gate: The $CoSi_2$ gates are fabricated using standard CMOS processes through source/drain (S/D) activation, with oxynitride as the gate dielectric. After inter-level dielectric (ILD) oxide deposition, CMP is performed to reduce the poly gate height in order to facilitate simultaneous silicidation of the gate, source and drain after ILD removal.

Tungsten Gate: A replacement gate approach is used in which, a sacrificial gate oxide (sac ox) and poly with a nitride hardmask (used to prevent silicidation) are used to define the device structures. After S/D activation and silicidation, an ILD layer is deposited and planarized by CMP to open the top surface of the poly. The poly in the gate and sac ox are removed by etching. The gate oxide/oxynitride dielectric and CVD W [1] are then deposited followed by CMP planarization and back end processing

3. Results and Discussions

Cobalt Silicide Gate: Fig. 1 shows a TEM cross section of $CoSi_2$ gate on a 1.5 nm oxynitride dielectric, demonstrating complete silicidation of the poly gate with no apparent Co and oxynitride interactions. Fig. 2 shows the nFET inversion capacitance for poly gated and $CoSi_2$ gated devices with the same gate dielectric showing elimination of 0.5 nm poly depletion. The Tinv for $CoSi_2$ gated device is ~1.7 nm, better than previously reported data with NiSi [2]. $CoSi_2$ and poly gated device transconductance measurements are shown in Fig. 3 revealing a Gm increase of 30% for $CoSi_2$ which correlates well with the lower Tinv for the silicide. Fig. 4 is the sub-threshold characteristics of n and pFETs with $CoSi_2$ and poly gates, with a sub-threshold slope of ~85 mV/decade indicating low interface state densities. Fig. 5 shows the superior time to breakdown characteristics of $CoSi_2$ devices when compared to poly devices for a given stress voltage and lower Tinv. This indicates that cobalt is not reacting with or penetrating the oxynitride dielectric. The $CoSi_2$ gate breakdown is 250 mV lower than comparable poly gated devices with 0.5 nm higher Tinv.

Tungsten Gate: Fig. 1b shows a cross-sectional TEM image of a replacement gate device with a W/2 nm oxide gate stack that exhibits smooth interfaces. Inversion C-V curves (Fig. 6) show a tight distribution for devices measured across the wafer (pFET Tinv~2.0 nm). Fig. 7 displays Id vs. Vg for W/oxide devices with sub-threshold slopes of ~85 mV/decade obtained for different channel lengths, ranging from 0.1 to 10 μm, demonstrating good functionality of these short-channel replacement gates. Lowest Tinv of ~1.8nm was obtained on W/oxynitride devices (Fig. 9). Differences in Vts are observed for oxide and oxynitride dielectrics with W gates (Figs. 6- 9) and can be attributed to the introduction of positive charge from nitrogen in the oxynitride and/or effect of PMA's. Ig vs. Tinv (Fig. 10) measured at 1.2 V, for W and poly gated oxynitride devices indicate lower Ig for W for the same Tinv. The leakage reduction corresponds to a 0.2 nm Tinv gain compared with the same poly gated oxynitride thickness. While pFET mobility is comparable for W & poly gated devices (Fig. 11), a degradation is observed in the peak nFET mobility of W gated devices (Fig. 12). This trend remains true independent of dielectric used, with peak nFET mobility degradation more pronounced for oxynitride. It is however, interesting to note that at higher inversion charge densities (corresponding to higher effective fields), the nFET mobility is comparable for W & poly

4. Conclusions

We have demonstrated metal gated conventional dielectric MOSFETs using a standard silicidation process for gate $CoSi_2$ formation and a replacement gate process for W. We report on the lowest metal gated /oxynitride Tinv of 1.7 nm (with $CoSi_2$) and 1.8 nm (with W). W gated devices show pFET mobilities comparable to Poly, while nFET mobilities are degraded at the peak but comparable with poly at high fields.

References

[1] D.A. Buchanan et al., Appl. Phys. Lett. 73, 1676 (1998)

[2] W. P. Maszara et al., IEDM Tech Digest, p. 367 (2002)

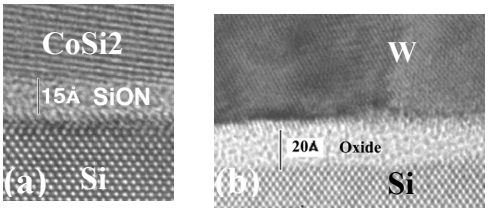


Fig. 1. TEM cross-sections of (a) $CoSi_2$ gate on 15Å Si-oxynitride and (b) W/20A SiO_2 gate stack

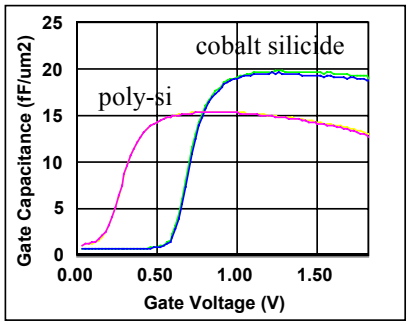


Fig. 2 Inversion C-V for n+ poly and $CoSi_2$ gate

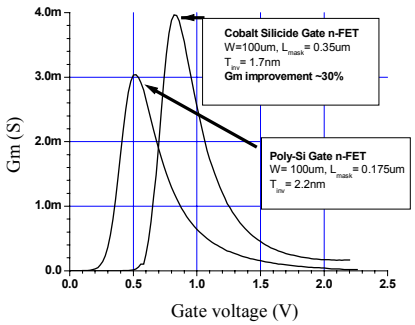


Fig. 3 Transconductance comparison between $CoSi_2$ and poly gated devices

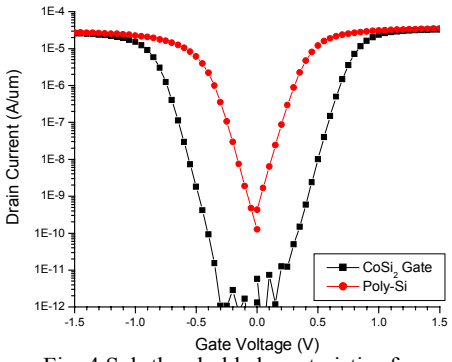


Fig. 4 Sub-threshold characteristics for $CoSi_2$ and poly gates

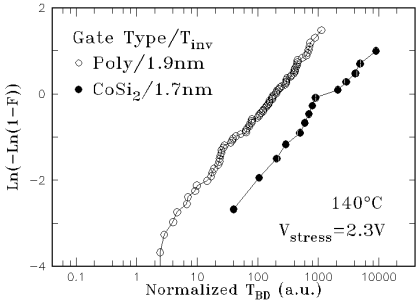


Fig. 5 Better time to breakdown characterist for $CoSi_2$ compared to poly gated devices

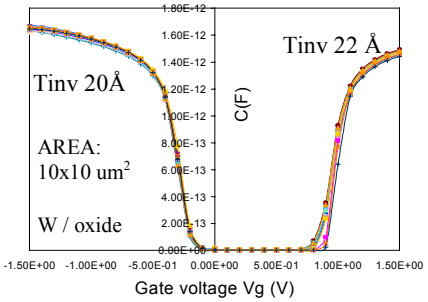


Fig. 6 Inversion CV curves for W/ oxide p-FETs and n-FETs

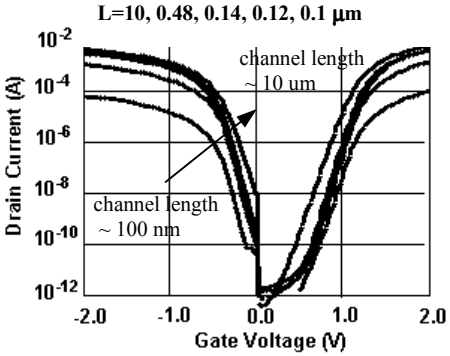


Fig. 7 W/oxide Id vs. Vg curves

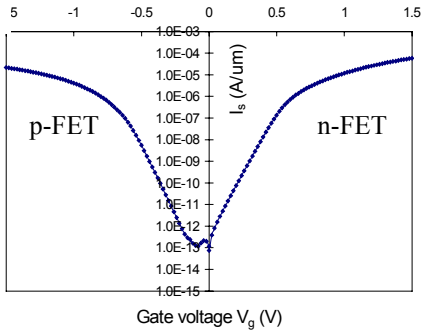
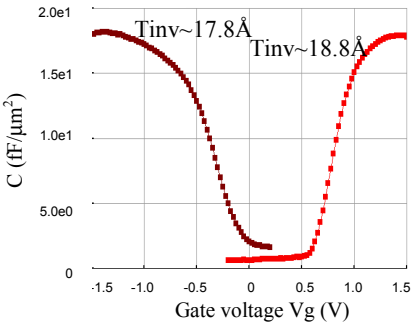


Fig. 8 W/oxynitride Id vs. Vg curves



oxynitride p-FETs and n-FETs

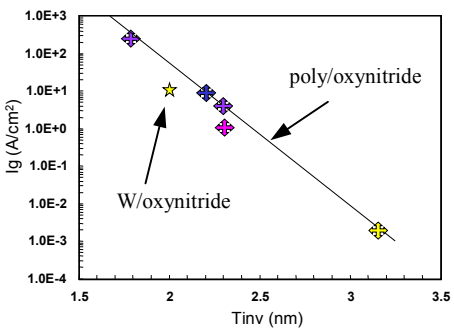


Fig. 10 Ig vs. Tinv comparing poly / W gated devices

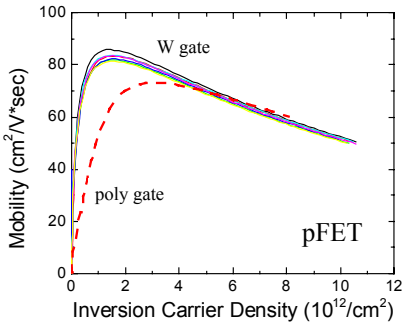


Fig. 11 W and poly gate p-FET mobility

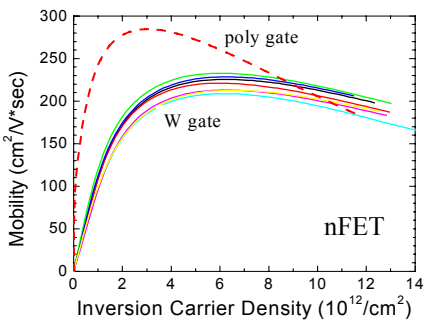


Fig. 12 W and poly gate n-FET mobility