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New Dual Metal Gate by Using WSi_x for nMOS and Pt-alloyed WSi_x for pMOS

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1. Introduction

As MOSFET gate lengths are scaled down to the 20nm regime or beyond, gate oxide thickness is required to be thinned to below 1nm. Metal gate is attractive material, since effective gate oxide thickness (estimated from inversion capacitance) can be thinner by more than 0.2nm as compared with that of poly-Si gate, thereby increasing MOSFETs drive current. Most important issue of metal gate is work function control of metal. This means so-called dual metal gate is needed in order to realize metal gate CMOSFETs with low Vth less than about 0.4V. Many dual metal gate processes were reported such as nitrogen ion implantation into Mo films [1], Ni fully silicide process [2]. However, nitrogen ion implantation process has a problem of channeling of nitrogen through a metal film and implantation into MOSFET channel region. On the other hands, Ni fully silicide process, there will be a problem of Ni diffusivity in Si and SiO_2 during post thermal processing.

In this paper, a new dual metal gate process is proposed. In this process, we applied a WSi_x film for a nMOS because of its appropriate work function of 4.45eV. In a pMOS, the WSi_x film was alloyed with an additional Pt film and work function of the WSi_x film was successfully converted into relatively higher value of 4.75eV.

2. Experimental

Figure 1 illustrates proposed dual metal gate structure and process using Pt/WSi_x stacked layer. A Pt film is selectively formed at only pMOS region, after a WSi_x film is deposited at both of nMOS and pMOS regions. A Pt/WSi_x stacked layer at pMOS region is converted into a Pt-alloyed WSi_x film ($Pt_xW_ySi_z$) by annealing, and dual metal gate are formed WSi_x for n-type MOSFET, Pt-alloyed WSi_x ($Pt_xW_ySi_z$) for p-type MOSFET, respectively.

In order to examine electrical properties, MOS capacitors were fabricated. Firstly, 100nm thermal SiO_2 field region was formed and 5-10 nm gate oxide films were thermally grown on p-type (100)Si substrates. Secondly, 25-100 nm $WSi_{2.8}$ films were deposited by DC magnetron sputtering and patterned by dry etching. Then, 100 nm Pt films were deposited by DC magnetron sputtering after removal of native SiO_2 on $WSi_{2.8}$ films by diluted HF wet etching. In some sample, an additional Ti or TiN cap layer was deposited after Pt film deposition. Annealing was carried out at 600°C for 60min in order to react $WSi_{2.8}$ film with Pt film. In order to remove unreacted cap/Pt layer, selective cap/Pt wet etching was carried out by using aqua regia. Finally, forming gas annealing was carried out at 450°C for 30min in a gas mixture of H_2 and N_2. These samples were characterized by X-ray diffraction (XRD), scanning electron microscope (SEM), transmission electron microscope (TEM), energy dispersive X-ray analysis (EDX). Electrical measurements such as C-V curve and gate leakage characteristics were carried out.

3. Results and Discussion

Figure 2 shows post-annealing temperature dependence of gate leakage current of $WSi_{2.8}$ gate capacitors. It is clear that gate leakage current is increased by post-annealing at above 700°C. This means thermal budget of post-annealing temperature must be less than 700°C in case of using WSi_x as a gate material. Figures 3 (a) and (b) show SEM images of $Pt/WSi_{2.8}$ gates after 600°C annealing, (a) without cap layer and (b) with Ti cap layer, respectively. It was found that surface morphology was degraded in the case of $Pt/WSi_{2.8}$ gates without cap layer. On the other hand, smooth surface was obtained by using cap layer. Cap layer is very effective in improving the surface morphology.

In order to examine Pt distribution, two dimensional analysis of EDX was carried out. Figures 4 (a) and (b) show TEM and EDX images of $Pt/WSi_{2.8}$ gate with Ti cap, (a) as deposition and (b) after post-annealing at 600°C for 60min, respectively. From TEM images, Pt adequately reacts with $WSi_{2.8}$ at 600°C. And it is clear that Pt diffuses homogeneously to the interface of WSi_x and gate oxide after 600°C post-annealing. In order to examine crystallinity of Pt-alloyed WSi_x, XRD measurement was carried out. Figure 5 shows XRD spectra of $Ti/Pt/WSi_{2.8}$, $Pt/WSi_{2.8}$ and $WSi_{2.8}$ films after annealing at 600°C for 60min. The XRD spectra indicate that Pt is transformed to PtSi regardless of cap layer.

In order to compare the electrical property of $Pt/WSi_{2.8}$ gate electrodes between with and without cap layer, C-V curve and gate leakage characteristics were measured as shown in Fig. 6 (a) and (b). Cap layer dependence of flat band voltage and gate leakage characteristics was not found. And gate leakage current of $Pt/WSi_{2.8}$ gates was not degraded as compared with that of $WSi_{2.8}$ gate. In order to estimate work functions of gate electrodes, gate oxide thickness dependence of flat band voltage was investigated as shown in Fig. 6 (c). It was found that work function of $Pt/WSi_{2.8}$ gate (Pt-alloyed $WSi_{2.8}$ gate) was about 4.70eV regardless of cap layer, and $WSi_{2.8}$ gate was about 4.45eV.

WSi_x thickness dependence of work function was examined, since Pt at the interface of gate electrode and gate oxide must be controlled by WSi_x thickness. Figures 7 (a), (b) and (c) show $WSi_{2.8}$ thickness dependence of electrical characteristics of $Pt/WSi_{2.8}$ gate capacitors with TiN cap. (a) C-V curve, (b) gate leakage characteristics, (c) work function (estimated from gate oxide thickness dependence of flat band voltage), respectively. Interface trap density and gate leakage characteristics don't depend on $WSi_{2.8}$ thickness. And work function is slightly increased with decrease of $WSi_{2.8}$ thickness. Work function of thinnest $WSi_{2.8}$ (25nm) sample is about 4.75eV. These work function results clearly show that WSi_x can be used in n-type MOSFET and Pt-alloyed WSi_x gate can be used in p-type MOSFET.

4. Conclusion

A new dual metal gate process is proposed. Work function of $WSi_{2.8}$ gate was successfully converted from 4.45eV into 4.75eV by alloying a $WSi_{2.8}$ film with an additional Pt film. The dual metal gate using $WSi_{2.8}$ (nMOS) and Pt-alloyed $WSi_{2.8}$ (pMOS) will realize the CMOSFETs with low Vth at least less than 0.4V.

Acknowledgments

The authors would like to thank Mr. T. Saito, Mr. K. Nakajima for valuable discussion.

References

[1] Pushkar Ranade *et al.*, IEDM Tech. Dig. (2002), p. 363.
[2] W. P. Maszara *et al.*, IEDM Tech. Dig. (2002), p. 367.

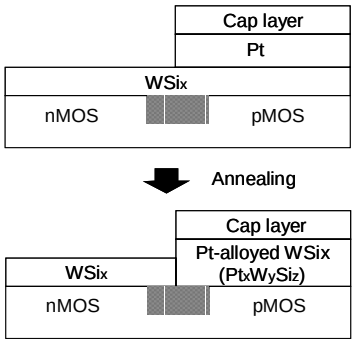


Fig. 1 : Proposed dual metal gate structure and process

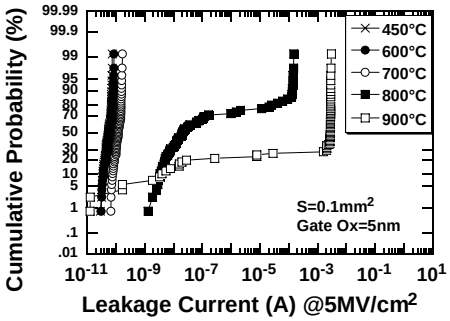


Fig. 2 : Annealing temperature dependence of gate leakage current of $WSi_{2.8}$ gate electrodes.

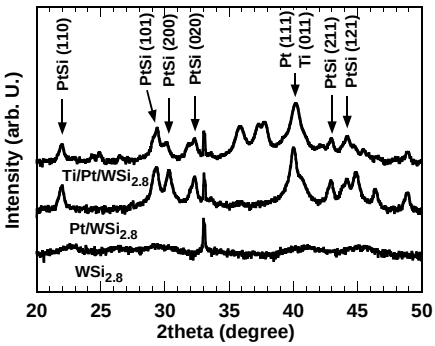


Fig. 5 : XRD spectra of Ti/ $Pt/WSi_{2.8}$, $Pt/WSi_{2.8}$ and $WSi_{2.8}$ films annealed at 600°C for 60min.

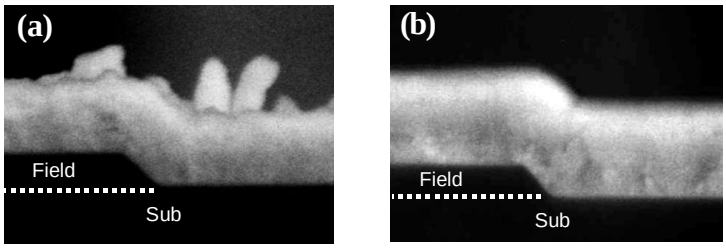


Fig. 3 : SEM Image of $Pt/WSi_{2.8}$ (100/100nm) gate after annealed at 600°C for 60min. (a) w/o cap, (b) with Ti cap (60nm), respectively.

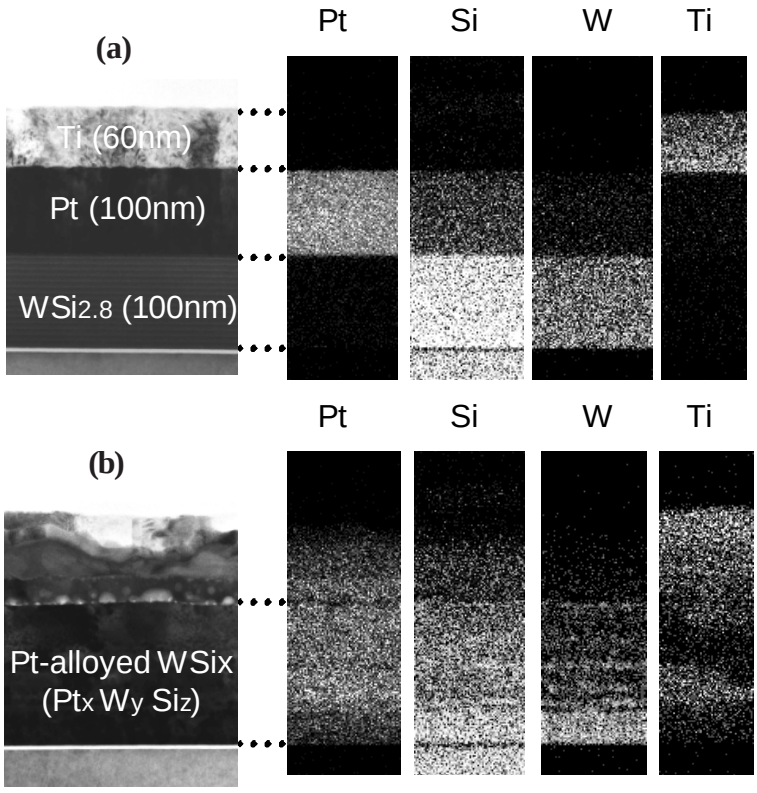
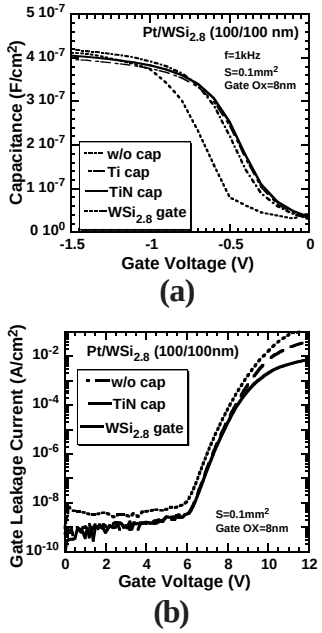


Fig. 4 : TEM images and Pt, Si, W and Ti EDX Images of $Pt/WSi_{2.8}$ (100/100nm) gate with Ti cap (60nm). (a) as deposition, (b) annealed at 600°C for 60min, respectively.



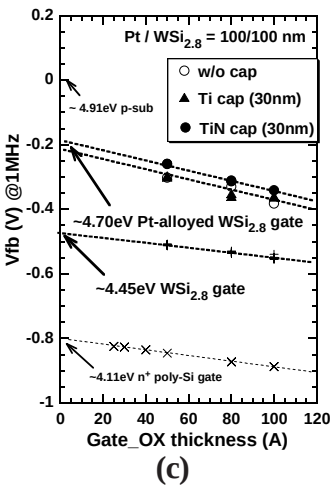
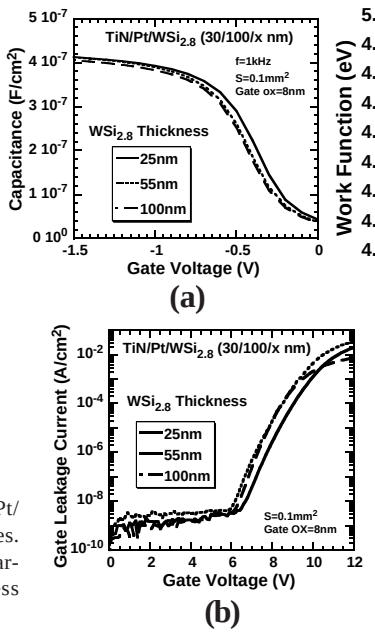


Fig. 6 : Cap layer dependence of $Pt/WSi_{2.8}$ (100/100nm) gate electrodes. (a) C-V curve, (b) gate leakage characteristics, (c) gate oxide thickness dependence of Vfb, respectively.



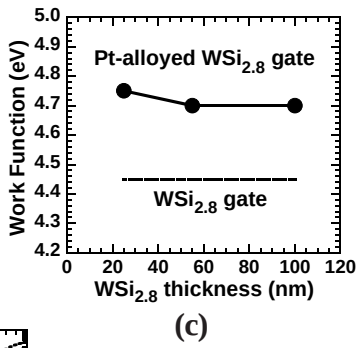


Fig. 7 : $WSi_{2.8}$ thickness dependence of $Pt/WSi_{2.8}$ (100/x nm) gate electrodes with TiN cap (30nm). (a) C-V curve, (b) gate leakage characteristics, (c) work function, respectively.