New Dual Metal Gate by Using WSi\textsubscript{x} for nMOS and Pt-alloyed WSi\textsubscript{x} for pMOS

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1. Introduction
As MOSFET gate lengths are scaled down to the 20nm regime or beyond, gate oxide thickness is required to be thinned to below 1nm. Metal gate is attractive material, since effective gate oxide thickness (estimated from inversion capacitance) can be thinner by more than 0.2nm as compared with that of poly-Si gate, thereby increasing MOSFETs drive current. Most important issue of metal gate is work function control of metal. This means so-called dual metal gate is needed in order to realize metal gate CMOSFETs with low Vth less than about 0.4V. Many dual metal gate processes were reported such as nitrogen ion implantation into Mo films [1], Ni fully silicided process [2]. However, nitrogen ion implantation process has a problem of channeling of nitrogen through a metal film and implantation into MOSFET channel region. On the other hands, Ni fully silicided process, there will be a problem of Ni diffusivity in Si and SiO\textsubscript{2} during post thermal processing.

In this paper, a new dual metal gate process is proposed. In this process, we applied a WSi\textsubscript{2.8} film for a nMOS because of its appropriate work function of 4.45eV. In a pMOS, the WSi\textsubscript{2.8} film was alloyed with an additional Pt film and work function of the WSi\textsubscript{2.8} film was successfully converted into relatively higher value of 4.75eV.

2. Experimental

Figure 1 illustrates proposed dual metal gate structure and process using Pt/WSi\textsubscript{2.8} stacked layer. A Pt film is selectively formed at only pMOS region, after a WSi\textsubscript{2.8} film is deposited at both of nMOS and pMOS regions. A Pt/WSi\textsubscript{2.8} stacked layer at pMOS region is converted into a Pt-alloyed WSi\textsubscript{2.8} film (Pt\textsubscript{(pMOS)}, WSi\textsubscript{2.8}) by annealing, and dual metal gate are formed WSi\textsubscript{2.8} for n-type MOSFET, Pt-alloyed WSi\textsubscript{2.8} (Pt\textsubscript{(nMOS)}, WSi\textsubscript{2.8}) for p-type MOSFET, respectively.

In order to examine electrical properties, MOS capacitors were fabricated. Firstly, 100nm thermal SiO\textsubscript{2} field region was formed and 5-10 nm gate oxide films were thermally grown on p-type (100)Si substrates. Secondly, 25-100 nm WSi\textsubscript{2.8} films were deposited by DC magnetron sputtering and patterned by dry etching. Then, 100 nm Pt films were deposited by DC magnetron sputtering after removal of native SiO\textsubscript{2} on WSi\textsubscript{2.8} films by diluted HF wet etching. In some sample, an additional Ti or TiN cap layer was deposited after Pt film deposition. Annealing was carried out at 600°C for 60min in case of using WSi\textsubscript{2.8} as a gate material. Figures 7 (a) and (b) show SEM images of Pt/WSi\textsubscript{2.8} gates after 600°C annealing. (a) without cap layer and (b) with Ti cap layer, respectively. It was found that surface morphology was degraded in the case of Pt/WSi\textsubscript{2.8} gates without cap layer. On the other hand, smooth surface was obtained by using cap layer. Cap layer is very effective in improving the surface morphology.

In order to examine Pt distribution, two dimensional analysis of EDX was carried out. Figures 4 (a) and (b) show TEM and EDX images of Pt/WSi\textsubscript{2.8} gate with Ti cap, (a) as deposition and (b) after post-annealing at 600°C for 60min, respectively. From TEM images, Pt adequately reacts with WSi\textsubscript{2.8} at 600°C. And it is clear that Pt diffuses homogeneously to the interface of WSi\textsubscript{2.8} and gate oxide after 600°C post-annealing. In order to examine crystallinity of Pt-alloyed WSi\textsubscript{2.8}, XRD measurement was carried out. Figure 5 shows XRD spectra of Ti/Pt/WSi\textsubscript{2.8}, Pt/WSi\textsubscript{2.8} and WSi\textsubscript{2.8} films after annealing at 600°C for 60min. The XRD spectra indicate that Pt is transformed to PtSi regardless of cap layer.

In order to compare the electrical property of Pt/WSi\textsubscript{2.8} gate electrodes between with and without cap layer, C-V curve and gate leakage characteristics were measured as shown in Fig. 6 (a) and (b) with Ti cap layer. Cap layer dependence of flat band voltage and gate leakage characteristics was not found. Gate leakage current of Pt/WSi\textsubscript{2.8} gates was not degraded as compared with that of WSi\textsubscript{2.8} gate. In order to estimate work functions of gate electrodes, gate oxide thickness dependence of flat band voltage was investigated as shown in Fig. 6 (c). It was found that work function of Pt/WSi\textsubscript{2.8} gate (Pt-alloyed WSi\textsubscript{2.8} gate) was about 4.70eV regardless of cap layer, and WSi\textsubscript{2.8} gate was about 4.45eV.

WSi\textsubscript{2.8} thickness dependence of work function was examined, since Pt at the interface of gate electrode and gate oxide must be controlled by WSi\textsubscript{2.8} thickness. Figures 7 (a), (b) and (c) show WSi\textsubscript{2.8} thickness dependence of electrical characteristics of Pt/WSi\textsubscript{2.8} gate capacitors with PtTi cap. (a) C-V curve, (b) gate leakage characteristics, (c) work function (estimated from gate oxide thickness dependence of flat band voltage), respectively. Interface trap density and gate leakage characteristics don’t depend on WSi\textsubscript{2.8} thickness. And work function is slightly increased with decrease of WSi\textsubscript{2.8} thickness. Work function of thinnest WSi\textsubscript{2.8} (25nm) sample is about 4.75eV. These work function results clearly show that WSi\textsubscript{2.8} can be used in n-type MOSFET and Pt-alloyed WSi\textsubscript{2.8} gate can be used in p-type MOSFET.

4. Conclusion
A new dual metal gate process is proposed. Work function of WSi\textsubscript{2.8} gate was successfully converted from 4.45eV into 4.75eV by alloying a WSi\textsubscript{2.8} film with an additional Pt film. The dual metal gate MOSFET and Pt-alloyed WSi\textsubscript{2.8} gate can be used in p-type MOSFET.

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References
Fig. 1: Proposed dual metal gate structure and process.

Fig. 2: Annealing temperature dependence of gate leakage current of WSi2.8 gate electrodes.

Fig. 3: SEM Image of Pt/WSi2.8 (100/100nm) gate after annealed at 600°C for 60min. (a) w/o cap, (b) with Ti cap (60nm), respectively.

Fig. 4: TEM images and Pt, Si, W and Ti EDX Images of Pt/WSi2.8 (100/100nm) gate with Ti cap (60nm). (a) as deposition, (b) annealed at 600°C for 60min, respectively.

Fig. 5: XRD spectra of Ti/Pt/WSi2.8, Pt/WSi2.8 and WSi2.8 films annealed at 600°C for 60min.

Fig. 6: Cap layer dependence of Pt/WSi2.8 (100/100nm) gate electrodes. (a) C-V curve, (b) gate leakage characteristics, (c) gate oxide thickness dependence of Vfb, respectively.

Fig. 7: WSi2.8 thickness dependence of Pt/WSi2.8 (100/x nm) gate electrodes with TiN cap (30nm). (a) C-V curve, (b) gate leakage characteristics, (c) work function, respectively.