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Highly Selective Etching of Ta/TaNx Metal Electrode to Si_3N_4 Gate Dielectric Employing $SiCl_4$–NF_3 Gas Mixture Plasma

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Abstract

We have developed a new etching technology for metal gate electrode with high selectivity to Si_3N_4 dielectric that is more than 100. Dry etching of Tantalum (Ta) and Tantalum Nitride (TaNx) electrodes, not only over thin SiO_2, but also over thin Si_3N_4 gate dielectric, is succeeded by employing a proper ratio of $SiCl_4$-NF_3 gas mixture plasma.

In this paper, we also demonstrate excellent characteristics of MOSFET and MNSFET (Metal-Nitride-Semiconductor) devices using low-resistivity TaNx/*bcc*-Ta/TaNx stacked metal gate.

Introduction

Aggressive scaling down of MOS devices has required adopting metal gate electrode because of their low-resistivity, no boron penetration and no gate depletion unlike polysilicon. Therefore, etching process of metal electrode with high selectivity to gate dielectric is one of key technologies for manufacturing of ultra-scaled MOS devices.

We have already proposed metal gate FD-SOI MOS device technologies using low-resistivity TaNx/*bcc*-Ta/TaNx stacked electrode over SiO_2 [1] and Si_3N_4 [2] gate dielectric. We employed Cl_2, $SiCl_4$, or SF_6 gases for metal gate etching process, however, the selectivity and the anisotropy are insufficient for mass-production.

This paper reports on the highly selective etching of Ta and TaNx, not only over thin SiO_2, but also over thin Si_3N_4 gate dielectric, employing a proper ratio of $SiCl_4$-NF_3 gas mixture plasma. Excellent characteristics of MOS FET and MNSFET devices using low-resistivity TaNx/*bcc*-Ta/TaNx stacked metal gate are also demonstrated.

Experimental

Experiments were carried out in a conventional ICP etcher. Selectivity was examined by using 4 kinds of films; sputtered Ta with Xe gas [3], reactive-sputtered TaNx with Xe-N_2 gas mixture, thermal-SiO_2, and HDP-CVD Si_3N_4. $SiCl_4$ and NF_3 gas mixture was used as an etching gas without dilution. The total flow rate was 100sccm and the pressure in the chamber was kept at 9 mtorr. The substrate temperature was controlled to 50℃.

FD-SOI MOSFET and MNSFET devices on SOI (~50nm) were fabricated with TaNx/*bcc*-Ta/TaNx stacked metal gate structure (Fig.1). Fig.2 compares resistivity of Ta on TaNx, Ta on SiO_2 and TaNx. Low resistivity below 20μohm-cm can be realized by using hetero-epitaxy technology [1]. SiO_2 gate dielectric for MOSFET was thermally grown at 750℃ (wet) and Si_3N_4 gate dielectric for MNSFET was directly grown on Si using microwave-excited plasma in NH_3-Ar gas mixture [4]. The stacked metal gate using a conventional resist mask was dry-etched by 2 steps. CF_4-NF_3 gas mixture was used for high-throughput during main-etching step and $SiCl_4$-NF_3 gas mixture was used for selectivity to dielectrics during end-point and over-etching steps.

Source/Drain region was formed by Ion-Implantation and annealing at 550℃ using Solid-Phase-Epitaxy (SPE) technique [5]. Process flow for these devices is shown in Fig.3. Details of FD-SOI device fabrication except for gate etching are described in [1,2].

Results and Discussion

Fig.4 shows Ta, TaNx, SiO_2 and Si_3N_4 etching rates as a function of gas mixture ratio [=NF_3/($SiCl_4$+NF_3)]. SiO_2 and Si_3N_4 etching rates are relatively low within range of 5%~20%. Ta and TaNx selectivity to dielectric that are calculated from Fig.4 are shown in Figs.5 and 6, respectively. In the both case, the selectivity to Si_3N_4 are higher than that to SiO_2, which are more than 100. While we tried lower bias power case, we have confirmed that there is a deposition layer on Si_3N_4 dielectric after over-etching step as shown in Fig.7. Then we speculate that this deposition layer formed by plasma polymerization based on $SiCl_4$-NF_3 chemistry causes the high selectivity to dielectrics.

Fig.8 shows a typical SEM photograph (as etching) of TaNx/*bcc*-Ta/TaNx stacked metal gate dry-etched with $SiCl_4$ -NF_3 gas mixture ratio of 10% during end-point step. The anisotropy is satisfactory (~89°) and LER (Line Edge Roughness) is quite small which is comparable with a conventional polysilicon gate. End-point for just etching of the stacked metal gate can be detected successfully on 288nm-wavelength signal as shown in Fig.9.

Figs.10 and 11 present typical Vg-Id characteristics of TaNx/*bcc*-Ta/TaNx stacked metal gate n-ch MOSFET (SiO_2 dielectric=2.90nm) and p-ch MNSFET (Si_3N_4 dielectric= 3.55nm; EOT is around 1.75nm) dry-etched with $SiCl_4$-NF_3 gas mixture ratio of 15% during end-point step. The subthreshold slopes less than 70mV/decade for the both devices have been achieved. Finally, Fig.12 exhibits off-current variation of p-ch MNSFET with 3.55nm-thickness Si_3N_4 in a 6-inch wafer (60 transistors). Tight distributions without any anomalous leakage current have been achieved.

Conclusion

Highly selective etching of Ta/TaNx electrode to Si_3N_4 and SiO_2 gate dielectrics employing $SiCl_4$-NF_3 gas mixture plasma has been developed.

In addition, we succeeded in fabricating TaNx/*bcc*-Ta/TaNx stacked metal gate FD-SOI devices with thinner dielectrics using a conventional gate structure.

References

[1] H. Shimada et al., IEEE T-ED, vol. 48, no.8, p. 1619 (2001)
[2] H. Shimada et al., VLSI Tech., p. 67 (2001)
[3] T. Ushiki et al., IRPS, p. 307 (1998)
[4] K. Sekine et al., IEEE T-ED, vol. 47, no.7, p. 1370 (2000)
[5] H. Shimada et al., IEDM, p. 881 (1995)

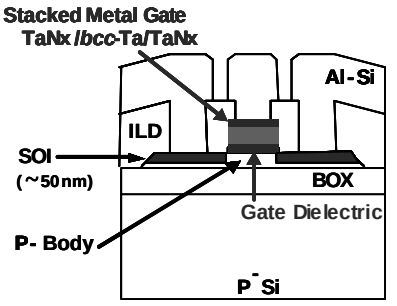

Fig.1 Cross sectional view of fabricated FD-SOI devices with *bcc*-Ta/TaNx metal gate. Top TaNx is introduced as a protective layer from oxidizing ambient.

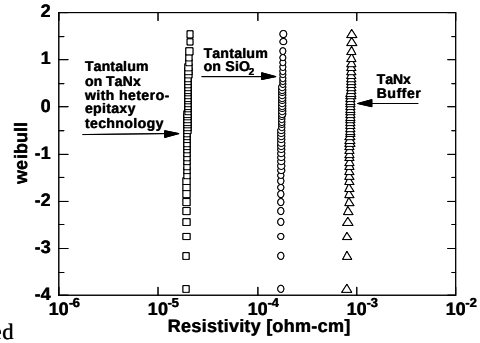

Fig.2 Resistivity distributions of sputtered Ta on TaNx, Ta on SiO_2 and TaNx buffer in a 6-inch wafer.

- SOI Island Mesa-Isolation (RIE)
- Dielectric Formation
  Direct Silicon-Nitride (Si_3N_4) Dielectric
  or *Conventional Thermal Wet Oxide*
- TaNx/*bcc*-Ta/TaNx Metal Gate Formation (SP)
- High-Selectivity Ta-Gate Dry-Etching (ICP)
- Source/Drain Implantation
- ILD Oxide Deposition (LTO)
- Low-Temperature SPE Activation (550℃)
- Metallization (Al-Cu 0.5%)
- Sintering (H_2=3%, 450℃)

Fig.3 Process sequence of fabricated FD-SOI devices with *bcc*-Ta/TaNx stacked metal gate featuring fully low-temperature processing.

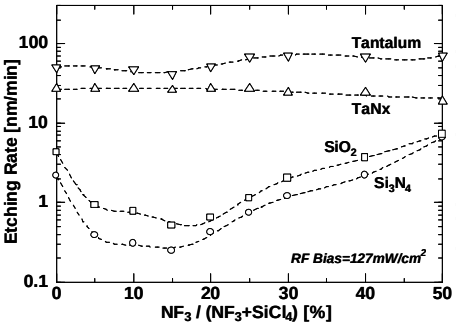

Fig.4 Etching rates of Ta, TaNx, SiO_2 and Si_3N_4 layer as a function of gas mixture ratio, $NF_3/(SiCl_4+NF_3)$.

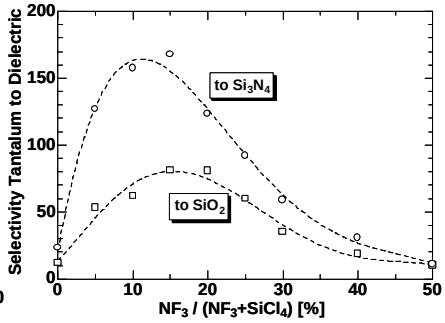

Fig.5 Selectivity of Ta to SiO_2 and Si_3N_4 dielectrics calculated from Fig.4.

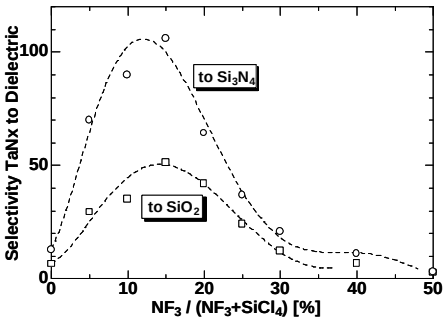

Fig.6 Selectivity of TaNx to SiO_2 and Si_3N_4 dielectrics calculated from Fig.4.

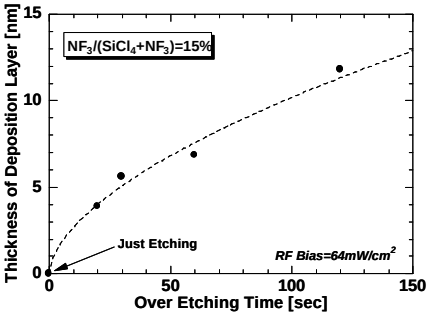

Fig.7 Thickness of deposition layer versus over-etching time in a case of low bias power. The data are measured by Nanospec and calibrated by GIXR.

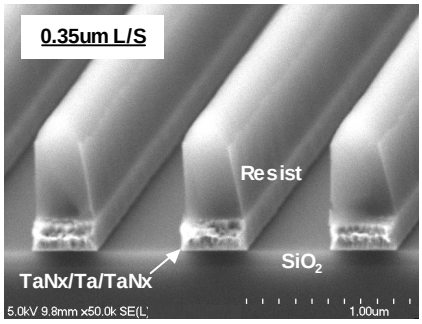

Fig.8 Bird-view TEM photograph of TaNx/*bcc*-Ta/TaNx metal gate on SiO_2 by 2-step etching. [M/E=CF_4-NF_3(30%) and EDP=$SiCl_4$-NF_3(10%)]

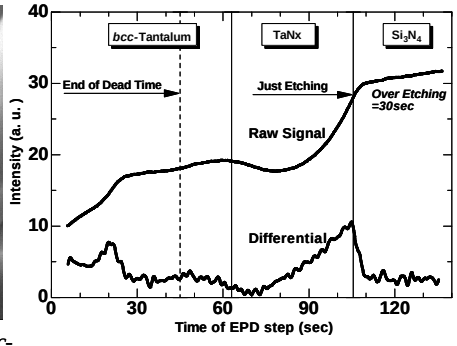

Fig.9 Typical EPD signal intensity on 288nm-wavelemgth during end-point step.

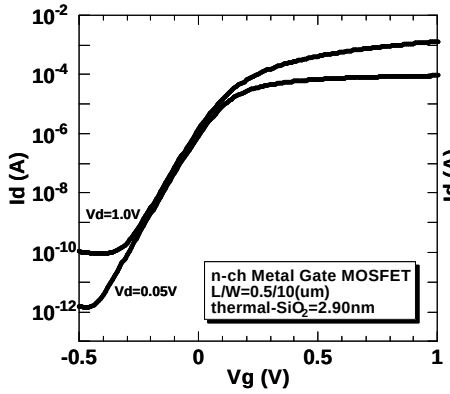

Fig.10 Subthreshold characteristics of Ta/TaNx metal gate FD-SOI nMOSFET.

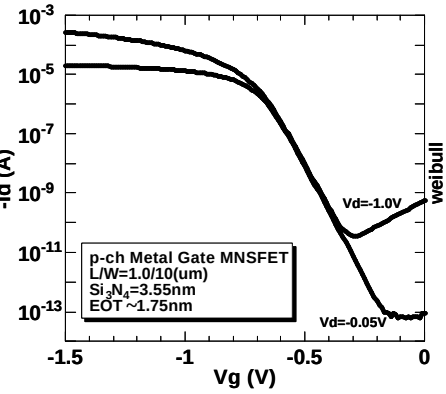

Fig.11 Subthreshold characteristics of Ta/TaNx metal gate FD-SOI pMNSFET. GIDL current is relatively higher due to a single drain structure and thinner EOT.

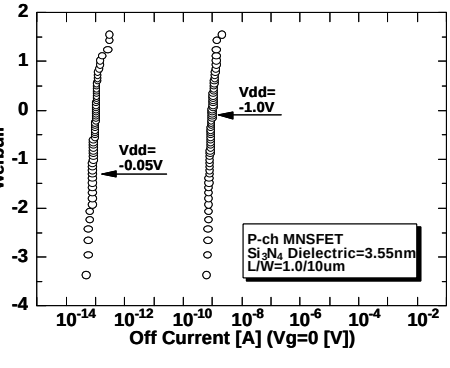

Fig.12 Off-current (Vg=0V) distributions of p-ch MNSFET with 3.55nm-thickness Si_3N_4 in a 6-inch wafer (60 transistors).