Highly Selective Etching of Ta/TaNx Metal Electrode to Si₃N₄ Gate Dielectric
Employing SiCl₄–NF₃ Gas Mixture Plasma

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Abstract
We have developed a new etching technology for metal gate electrode with high selectivity to Si₃N₄ dielectric that is more than 100. Dry etching of Tantalum (Ta) and Tantalum Nitride (TaNx) electrodes, not only over thin SiO₂, but also over thin Si₃N₄ gate dielectric, is succeeded by employing a proper ratio of SiCl₄–NF₃ gas mixture plasma.

In this paper, we also demonstrate excellent characteristics of MOSFET and MNSFET (Metal-Nitride-Semiconductor) devices using low-resistivity TaNx/bcc-Ta/TaNx stacked metal gate.

Introduction
Aggressive scaling down of MOS devices has required adopting metal gate electrode because of their low-resistivity, no boron penetration and no gate depletion unlike polysilicon. Therefore, etching process of metal electrode with high selectivity to gate dielectric is one of key technologies for manufacturing of ultra-scaled MOS devices.

We have already proposed metal gate FD-SOI MOS device technologies using low-resistivity TaNx/bcc-Ta/TaNx stacked electrode over SiO₂ [1] and Si₃N₄ [2] gate dielectric. We employed Cl₂, SiCl₄, or SF₆ gases for metal gate etching process, however, the selectivity and the anisotropy are insufficient for mass-production.

This paper reports on the highly selective etching of Ta and TaNx, not only over thin SiO₂, but also over thin Si₃N₄ gate dielectric, employing a proper ratio of SiCl₄–NF₃ gas mixture plasma. Excellent characteristics of MOS FET and MNSFET devices using low-resistivity TaNx/bcc-Ta/TaNx stacked metal gate are also demonstrated.

Experimental
Experiments were carried out in a conventional ICP etcher. Selectivity was examined by using 4 kinds of films; sputtered Ta with Xe gas [3], reactive-sputtered TaNx with Xe–N₂ gas mixture, thermal-SiO₂, and HDP-CVD Si₃N₄. SiCl₄ and NF₃ gas mixture was used as an etching gas without dilution. The total flow rate was 100sccm and the pressure in the chamber was kept at 9 mtorr. The substrate temperature was controlled to 50°C.

FD-SOI MOSFET and MNSFET devices on SOI (~50nm) were fabricated with TaNx/bcc-Ta/TaNx stacked metal gate structure (Fig.1). Fig.2 compares resistivity of Ta on TaNx, Ta on SiO₂ and TaNx. Low resistivity below 20μΩcm can be realized by using hetero-epitaxy technique [1]. SiO₂ gate dielectric for MOSFET was thermally grown at 750°C (wet) and Si₃N₄ gate dielectric for MNSFET was directly grown on Si using microwave-excited plasma in NH₃–Ar gas mixture [4]. The stacked metal gate using a conventional resist mask was dry-etched by 2 steps. CF₄–NF₃ gas mixture was used for high-throughput during main-etching step and SiCl₄–NF₃ gas mixture was used for selectivity to dielectrics during end-point and over-etching steps.

Source/Drain region was formed by Ion-Implantation and annealing at 550°C using Solid-Phase-Epitaxy (SPE) technique [5]. Process flow for these devices is shown in Fig.3. Details of FD-SOI device fabrication except for gate etching are described in [1,2].

Results and Discussion
Fig.4 shows Ta, TaNx, SiO₂ and Si₃N₄ etching rates as a function of gas mixture ratio [=NF₃/(SiCl₄+NF₃)]. SiO₂ and Si₃N₄ etching rates are relatively low within range of 5%~20%. Ta and TaNx selectivity to dielectric that are calculated from Fig.4 are shown in Figs.5 and 6, respectively. In the both case, the selectivity to Si₃N₄ are higher than that to SiO₂, which are more than 100. While we tried lower bias power case, we have confirmed that there is a deposition layer on Si₃N₄ dielectric after over-etching step as shown in Fig.7. Then we speculate that this deposition layer formed by plasma polymerization based on SiCl₄–NF₃ chemistry causes the high selectivity to dielectrics.

Fig.8 shows a typical SEM photograph (as etching) of TaNx/bcc-Ta/TaNx stacked metal gate dry-etched with SiCl₄–NF₃ gas mixture ratio of 10% during end-point step. The anisotropy is satisfactory (~89°) and LER (Line Edge Roughness) is quite small which is comparable with a conventional polysilicon gate. End-point for just etching of the stacked metal gate can be detected successfully on 288nm-wavelength signal as shown in Fig.9.

Figs.10 and 11 present typical Vg-Id characteristics of TaNx/bcc-Ta/TaNx stacked metal gate n-ch MOSFET (SiO₂ dielectric=2.90nm) and p-ch MNSFET (Si₃N₄ dielectric=3.55nm; EOT is around 1.75nm) dry-etched with SiCl₄–NF₃ gas mixture ratio of 15% during end-point step. The subthreshold slopes less than 70mV/decade for the both devices have been achieved. Finally, Fig.12 exhibits offset current variation of p-ch MNSFET with 3.55nm-thickness Si₃N₄ in a 6-inch wafer (60 transistors). Tight distributions without any anomalous leakage current have been achieved.

Conclusion
Highly selective etching of Ta/TaNx electrode to Si₃N₄ and SiO₂ gate dielectrics employing SiCl₄–NF₃ gas mixture plasma has been developed.

In addition, we succeeded in fabricating TaNx/bcc-Ta/TaNx stacked metal gate FD-SOI devices with thinner dielectrics using a conventional gate structure.

References
Stacked Metal Gate
Ta/TaNx Segment
Al-Si
SOI
(50nm)
Gate Dielectric
P- Body
P+ Body
ILD
Gate Oxide
Stacked Metal Gate
SOI
Fig.1 Cross sectional view of fabricated FD-SOI devices with bcc-Ta/TaNx metal gate. Top TaNx is introduced as a protective layer from oxidizing ambient.

Fig.2 Resistivity distributions of sputtered Ta on TaNx, Ta on SiO₂, and TaNx buffer in a 6-inch wafer.

Fig.3 Process sequence of fabricated FD-SOI devices with bcc-Ta/TaNx stacked metal gate featuring fully low-temperature processing.

Fig.4 Etching rates of Ta, TaNx, SiO₂ and Si₃N₄ layer as a function of gas mixture ratio, NF₅/(SiCl₄+NF₅).

Fig.5 Selectivity of Ta to SiO₂ and Si₃N₄ dielectrics calculated from Fig.4.

Fig.6 Selectivity of TaNx to SiO₂ and Si₃N₄ dielectrics calculated from Fig.4.

Fig.7 Thickness of deposition layer versus over-etching time in a case of low bias power. The data are measured by Nanospec and calibrated by GIXR.

Fig.8 Bird-view TEM photograph of TaNx/bcc-Ta/TaNx metal gate on SiO₂ by 2-step etching. [M/E=CF₂-NF₅(30%) and EDP=SiCl₂-NF₅(10%)]

Fig.9 Typical EPD signal intensity on 288nm-wavelength during end-point step.

Fig.10 Subthreshold characteristics of Ta/TaNx metal gate FD-SOI nMOSFET.

Fig.11 Subthreshold characteristics of Ta/TaNx metal gate FD-SOI pMOSFET. GIDL current is relatively higher due to a single drain structure and thinner EOT.

Fig.12 Off-current (Vgs=0V) distributions of p-ch MNSFET with 3.55nm-thickness Si₃N₄ in a 6-inch wafer (60 transistors).