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Ni-salicided Poly-Si/poly-SiGe Layered Gate Technology for 65nm-node CMOSFETs

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1. Introduction

Poly-SiGe is one of promising gate materials to be coordinated with high-k films because of its lower gate depletion and its preferable work function [1-2]. For 90 nm-node CMOSFETs, the Ge-content of poly-Si/poly-SiGe was reported to be suppressed less than 20% for stable Co-salicidation [3-4]. In 65 nm-node CMOSFETs, it would be possible to increase the Ge-content because Ni-salicide would be used and the silicidation temperature could be lowered.

In this paper, we will demonstrate a high Ge-content poly-Si/poly-SiGe layered gate stack with which both good morphology and stable Ni-salicidation is possible. The performance of L_{gate}=70 nm MOSFETs with this layering will also be reported.

2. Experimental

SiGe films are grown on 300 mm wafers with 2 or 3 nm-thick SiON by low-pressure chemical vapor deposition with a vertical tube using SiH_4 and 10%-H_2 diluted GeH_4, as source gases. A 5 nm-thick amorphous Si film is grown prior to SiGe deposition as a seed layer. The typical growth temperature was 475℃.

FETs were fabricated using a conventional CMOS process. After STI and n/p-well formations, a 2 nm-thick SiON gate was formed by Remote-Plasma-Oxidation followed by Nitridation. Poly-Si/SiGe gate electrodes were patterned by RIE. Thermal oxidation was done at 1000℃for 5s before extension- and halo-ion implantation. After a SiN sidewall formation and deep-S/D implantations, the dopant activation was carried out by a spike annealing at 1050℃, followed by a Ni-salicidation.

3. Results and Discussion

Fig. 1 shows the Ge-content dependence of the gate depletion. For PMOS, the ratio of inversion-capacitance (Cinv) to accumulation-capacitance (Cacc), increases with increasing the Ge-content up to 30%, and is then saturated. On the other hand, for NMOS, Cinv/Cacc is almost constant up to 30%, and decreases slightly for Ge-content higher than 30%. This result demonstrates that the optimum Ge-content is 30% for CMOS-fabrication.

However, the surface becomes rough as the Ge-content increases. Another concern about the morphology is the thickness dependence of the roughness. In order to secure stable silicidation, a poly-Si/SiGe layered structure is necessary [3]. Thus, the poly-SiGe should be thinner than 50 nm in order to keep a gate-height less than 100nm

. However, the morphology of SiGe-films gets worse as the SiGe-film becomes thinner. Figure 2 shows the thickness-dependence of morphology on the $Si_{0.7}Ge_{0.3}$ film. In contrast to good morphology for the 150 nm-thick film, a lot of voids are found in the 50 nm-thick film, and an island structure was observed for the 20 nm-thick film. The fact that the void is not observed in the thicker film (Fig. 2(a)) but observed in the thinner film (Fig. 2(b)) suggested that these voids have formed in a process tube after SiGe deposition due to its poor thermal stability. We found that good morphology could be obtained at pressure higher than 200 Pa or at pressure lower than 10 Pa (Fig. 3). A thin Si-cap (5 nm) deposited at the same temperature is helpful to suppress the surface migration resulting in better thermal stability. According to the XRD-measurement, high-pressure deposited film is amorphous. Figure 4 shows Si/SiGe layered structures actually fabricated for SiGe-films as shown in Fig. 3. Both films maintain the good morphology followed by the Si-deposition in higher temperatures.

SIMS measurements revealed that B diffusion in poly-SiGe is slower than that in poly-Si, and that in α -SiGe is much slower (Fig. 5). This result indicates that the B concentration of poly-SiGe at the gate electrode/SiON interface is lower than that in poly-Si. On the contrary, B-activation in poly-SiGe is faster than that in poly-Si, as shown in Fig. 6. These results mean that B is more effectively activated in poly-SiGe than in poly-Si.

Therefore, we fabricated CMOSFETs using a poly-Si/poly-SiGe layered gate and Ni-salicide with a gate length of 70 nm. A TEM photograph of the FET is shown in Fig. 7. Stable Ni-salicidation can be obtained over 300 mm, as shown in Fig. 8. Although the C-V and subthreshold Id-Vg characteristics were almost the same and showed no B penetration after annealing at 1000℃ for 5s (Fig. 9, 10), a lower Ioff was obtained, due to a larger band offset of SiGe, compared with poly-Si. As a result, a 35% larger drive current (295 uA/um) is obtained in the poly-SiGe gate FET, keeping the same Ioff of 3E-10A/um, as shown in Fig. 11.

4. Conclusion

It is shown that the optimum Ge-content for suppressing the gate depletion is 30%. We have found that both good morphology and enough B-concentration at a poly/gate -insulator interface can be achieved by poly-$Si_{0.7}Ge_{0.3}$ grown at a pressure less than 10 Pa. Stable Ni-salicidation over the 300 mm-wafer was confirmed on the poly-Si/poly-$Si_{0.7}Ge_{0.3}$. A high drive-current of 295 uA/um with the Ioff of 3E-10A/um was obtained on p-FETs with L_{gate}=70 nm using this layered gate structure.

References

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[3] H. Sato, et al., Mat. Res. Soc. Symp. Proc, K5. 10, (2001)
[4] H. S. Rhee, et al., Symp on VLSI Tech. Dig. 126 (2002)

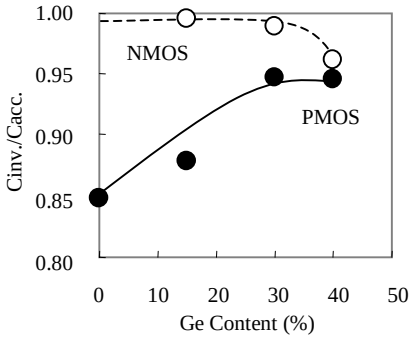

Fig. 1. Ge-content-dependence of the gate-depletion for NMOS and PMOS with 50nm α-Si/100nm-SiGe deposited at 475℃.

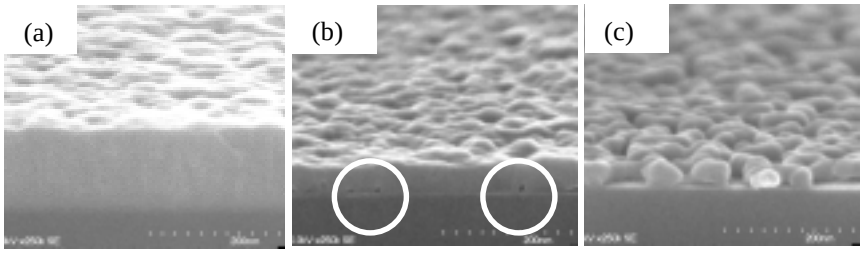

Fig. 2. Thickness dependence of $Si_{0.7}Ge_{0.3}$-flim morphology. Thickness of (a), (b), and (c) are 150nm, 50nm, and 20nm.

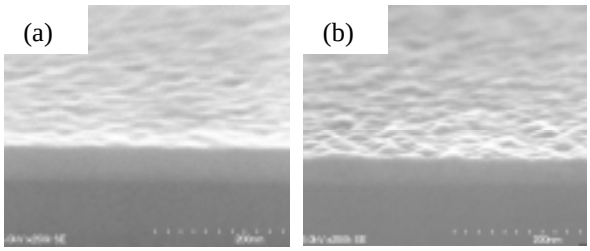

Fig. 3. Pressure dependence of $Si_{0.7}Ge_{0.3}$-flim morphology. (a) 200Pa, (b) 10Pa. Thickness is 50nm.

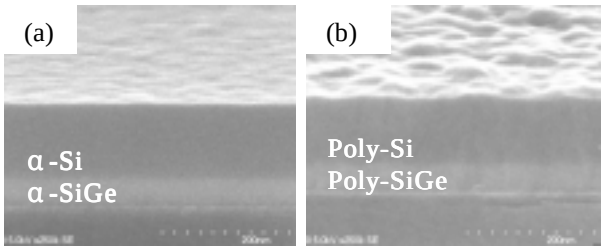

Fig. 4. Si/ $Si_{0.7}Ge_{0.3}$ layered structure for salicidation.
(a) α-SiGe followed by α-Si deposition at 530℃.
(b) Poly-SiGe followed by Poly –Si deposition at 620℃.

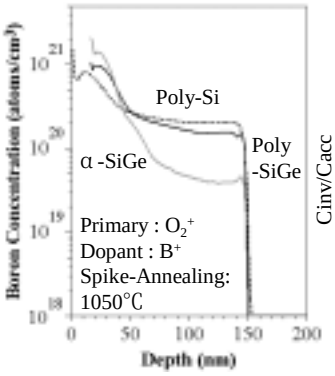

Fig. 5. SIMS-Profile of B-diffusion in poly-SiGe, α-SiGe and poly-Si.

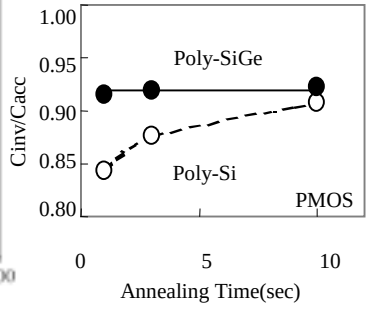

Fig. 6. Annealing-time dependence of B-activation in poly-SiGe and poly-Si. Annealing temperature = 1000℃

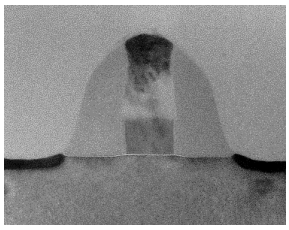

Fig. 7. Cross sectional TEM image of FET using Si/SiGe layered structure with Ni-salicidation. L_{gate}=70nm

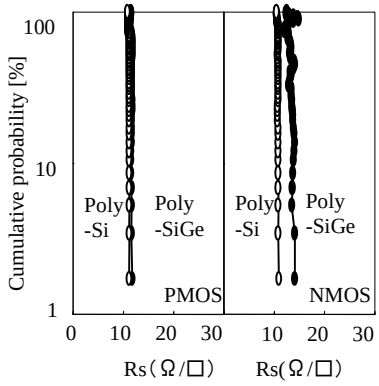

Fig. 8. Rs distributions of Ni-salicides with the poly-Si and poly-Si/poly-SiGe

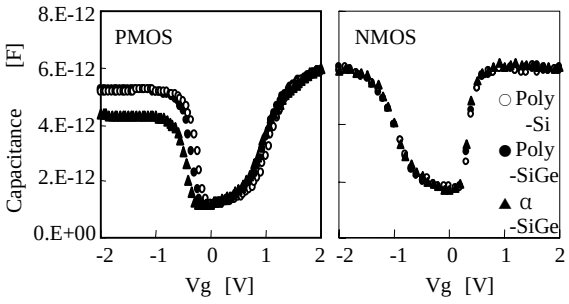

Fig. 9. C-V characteristics for P- and N-capacitor. Area=400um^2.

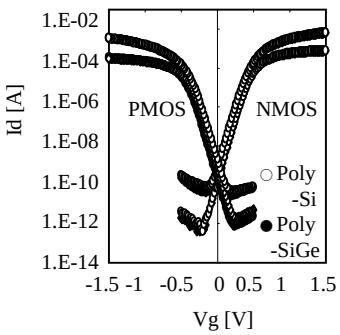

Fig. 10. Subthreshold Id-Vg characterristics of n/pFET
L / W = 90nm/10um,Vd=-1.2V and -0.05V.

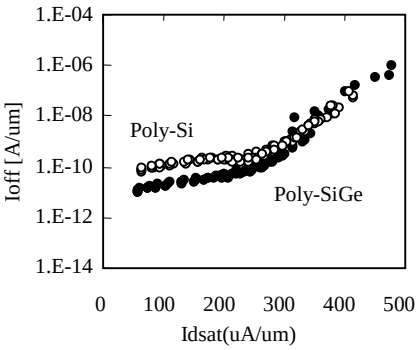

Fig. 11. Idsat-Ioff characteristics for pFET. Vg=Vd=-1.2V.