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Pre-amorphization and co-implantation suitability for advanced PMOS devices integration

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1. Introduction

The increasingly stringent requirements for ultra-shallow junctions (USJ) have led to the point where, for the 65nm technology node already, conventional implantation and spike annealing approaches cannot offer solutions for the desired USJ, especially for PMOS transistors. In the recent years special attention was given to pre-amorphization studies, co-implantations and fast ramp-up and ramp-down anneals to provide highly active and abrupt ultra-shallow junctions [1-4]. Furthermore, junction leakage and junction de-activation have become one of the main issues in integrating these USJ.

In this paper we show that using Ge pre-amorphization implants, properly tuned F co-implantation and fast ramp-up and ramp-down anneals, combined with a low temperature processing scheme, leads to a remarkable improvement in performance for PMOS devices.

2. Experimental

Implantation and anneal

From extensive studies (shown elsewhere, see ref.[2-4]) on optimizing PMOS junctions we showed that B USJs can be greatly improved by deep Ge pre-amorphization implants (to limit B channeling) combined with F co-implantation beyond boron's projected range and at the end-of-range (EOR) defects position. The presence of F (an interstitial diffuser) at the EOR, the highest Si interstitial gradient, leads to coupling of F with the interstitials, therefore reducing the B TED upon annealing. Fluorine implant fine-tuning is essential since this can overcome the major drawback of pre-amorphization, the presence of interstitial rich damage band at the EOR [5-8]. Additionally, a fast ramp-up and ramp-down is necessary to achieve the best optimized PMOS junctions [2-4]. The anneals were performed on the ASM Levitor tool, with a ramp-up rate of 800ºC/s and a ramp-down of 100ºC/s.

Fig. 1 shows the SIMS profiles for the reference B-only implant (0.5 keV, 7e14) and that for the optimized Ge + F + B (same B conditions) implant, annealed at 1070ºC. The optimized junction is shallower (X_j = 25.5nm @ C_B = 10^{18} at./cm^3), more abrupt (4.5 nm/decade) and highly activated (R_{sheet} = 606 Ohm/sq.), suitable for 65nm node device integration. Cross-section TEM studies showed that upon this type of anneals, all EOR defects were cured. We used these conditions for the source/drain extensions in a low temperature PMOS process flow. Furthermore, to achieve necessary overlap with the gate, various tilted implant angles (0º, 7º and 20º) were explored for the pre-amorphization step.

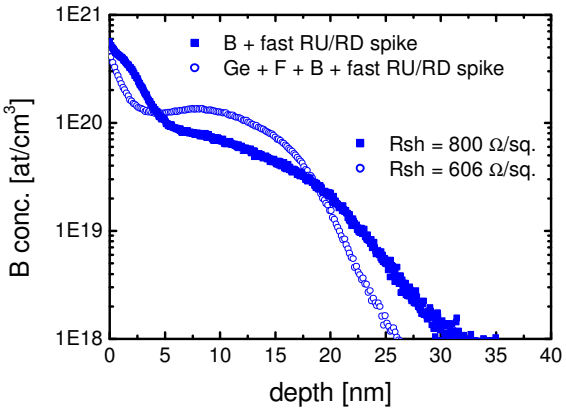

Fig. 1. Boron dopant SIMS profiles for the reference wafer condition (B implant and a 1070ºC Levitor spike) and the wafer with optimized conditions (Ge pre-amorphization + F co-implantation + B implant and 1070ºC Levitor spike)

Low temperature process flow

PMOS devices were realized using heavily nitrided oxide with an Equivalent Oxide Thickness (EOT = 1.4nm), and 100 nm doped poly-Si gates. To maintain the junctions' characteristics the process flow was designed such that,

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apart from the Levitor spike, all temperature steps are kept below 500ºC (i.e. minimize dopant diffusion and de-activation). The process flow after gate patterning is as follows:

- low tilt angle P pocket implant
- 10nm low T (PECVD, 400ºC) oxide offset spacers
- **extension implants (Ge + F + B)**
- low T (PECVD, 400ºC) oxide spacers
- source/drain implants
- **Levitor anneal**
- NiSi (< 450ºC)
- low T back-end processing

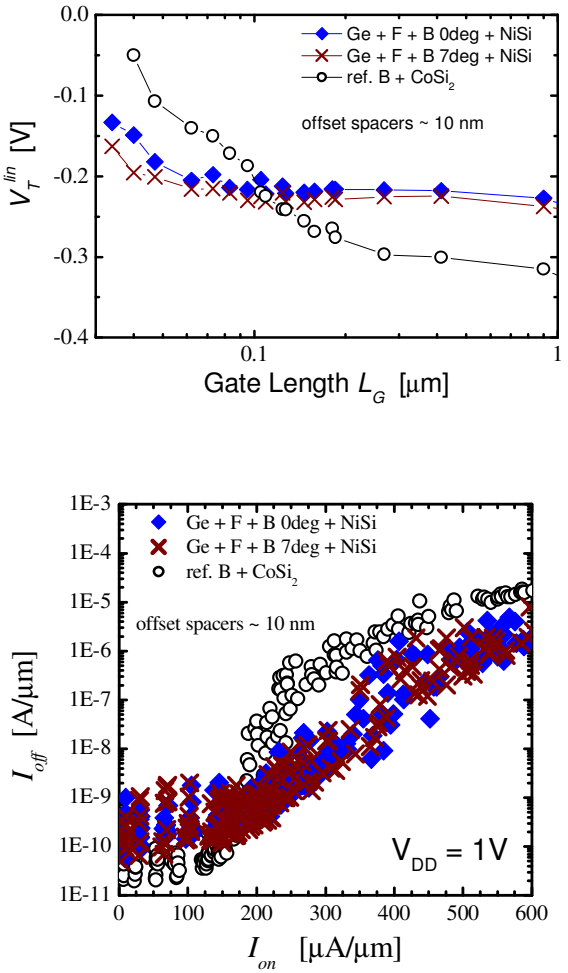

Fig. 2. Threshold voltage dependence on gate length (2a) and drive current vs. off-state current (2b) for the reference wafer (USJ B only + $CoSi_2$) and for wafers with two wafers with optimized USJ conditions (Ge pre-amorphization tilt angle conditions 0º or 7º and NiSi).

Low-temperature Plasma Enhanced CVD (PECVD) thin (10nm) oxide offset spacers were used to control the extensions – pocket combination by precisely tuning the extension position and the extension overlap with the gate [9]. NiSi was used for the silicidation step, in order to benefit from the lower thermal budget and lower contact resistance compared to $CoSi_2$.

3. Results

Fig. 2a illustrates the linear threshold voltage dependence on the gate length for the reference wafer (USJ B only + $CoSi_2$) and for two wafers with optimized USJ conditions, using 0º and 7º for Ge pre-amorphization implant and NiSi. All other conditions were identical for these three wafers. Excellent control of the V_T^{lin} is obtained by aggressive lateral profiling of the source/drain extensions using highly abrupt Ge pre-amorphization implant extensions in combination with no tilt highly doped P pocket implants. The activation step for both pocket and extension was done at the same time, at the Levitor anneal step. Furthermore, using 7° titled Ge pre-amorphization implant, slightly better control of the short channel effects can be achieved.

Fig. 2b shows the drive current versus off-state current for the same wafers as in Fig. 2a, at the supply voltage V_{DD} = 1V. For long channel length devices, the off-state leakage is slightly higher for the pre-amorphized wafers, possibly due to higher leakage caused by more abrupt junctions. However, at shorter gate length devices, the I_{on} – I_{off} trade-off is remarkably improved for the pre-amorphized junctions in combination with NiSi, yielding an Ion = 450 mA/µm at Ioff = 40nA/µm for devices with Lg ~ 50nm. No sign of B penetration was observed, in spite of the F implant (known to enhance penetration). Further optimization can be easily performed by adjusting the pocket implant conditions.

3. Conclusions

We have shown that the use of Ge pre-amorphized B junctions, with F co-implantation and in combination with a low temperature integration scheme greatly improves PMOS transistor performance, making those junctions suitable for integration into advanced technology nodes devices. Moreover, these junctions show great potential for integration in double-gate devices [10], where lateral abruptness is crucial for good device performance.

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References

[1] V. Meyssen et al. *Mat. Res. Soc. Symp. Proc.* **669** (2001)
[2] B.J. Pawlak et al. *IIT 2002, ECS 2003*
[3] R. Lindsay et al. *Mat. Res. Soc. Symp. Proc.* 2003
[4] C.J.J. Dachs et al., *USJ Workshop 2003*
[5] L.S. Robertson et al., *IEEE 2002,* p. 171
[6] J. Liu et al. *IEEE 1999*, pp. 951-954.
[7] N. Cowern et al. *Mat. Res. Soc. Symp. Proc.* 2003
[8] Duffy, to be published in *Appl. Phys. Lett.*
[9] R. Surdeanu et al. *ESSDERC 2001*
[10] H.S.P. Wong . *IEDM'98 Techn.Digest*, p.407