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On the Performance Advantage of undoped ultra thin-film FD-SOI MOSFETs

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Introduction

Ultra thin-film fully depleted SOI (FD-SOI) CMOS have many optimal advantages for ultra low-power applications. The advantages are the reduction of the junction capacitance and the suppression of the short-channel effect and so on. Furthermore, in order to apply this technology to an ultra high-speed application, a differential enhancement-depletion (ED)-CMOS/SOI circuit technology composed of undoped body depletion MOSFET (DMOS) is proposed [1]. However, the undoped body DMOS has a problem of poor control threshold voltage with gate length reduction caused by short channel effect. To improve this problem, source drain extension structure with pocket implantation apply to undoped body DMOS, and well suppress short channel effect and high drive capability is achieved. In this report, we demonstrate the performance of 0.15um ultra thin-film undoped body DMOS.

Results and discussion

Ultra thin-film FD-SOI MOSFET was fabricated using 0.15um technology. Fig.1A shows a cross section TEM image of Gate Length 0.15um SOI MOSFET. In this technology, offset-implanted source/drain extension with pocket implantation was adopted to suppress short channel effects as shown in Fig.1B. Modified LOCOS with SiN sidewall and thin cobalt salicide with contact hole etching prior to the second annealing [2] was used. The resistivity of source/drain region is less than 20ohm/square. The thickness of gate oxide, SOI and buried oxide layer are 2.5nm, 40nm and 200nm respectively.

Fig.2A shows the measured and simulated gate length dependence of the threshold voltage in the various doping concentration of the pocket region. In this simulation, 3-dimensional TCAD system (Enexss) developed in Semiconductor Leading Edge Technology was used. As shown figure, reverse short channel effect appears with increasing of pocket doping concentration. Since the threshold voltage of thin film FD-SOI mainly depends on impurities concentration in the body region, reverse short channel effect can be explained due to the increase in the ratio of the pocket region occupied in the body region with decreasing of channel length. Short channel effect can be suppressed by the optimizing of the pocket doping concentration as shown in Fig.2B. Furthermore, the undoped body DMOS makes it possible to adjust threshold voltage by using a back gate bias. Fig.2C shows the simulated dependence of the threshold voltage on the body doping concentration with various back gate bias. The influence of the backgate bias on the threshold voltage becomes small with increasing of body doping concentration. For the FD-SOI circuits composed of depletion and enhanced NMOS, the influence of back gate bias dose not affects to enhancement type.

The DC characteristic of both enhancement and depletion type NMOS are compared as shown in Fig.3. Short channel effect is well suppressed, and driving current capability of depletion type is about 1.5 times larger than that of enhancement type. The enhancement of current drive capability causes from the low threshold voltage and improvement in the mobility originated from reduction of the impurity scattering and the suppression of effective field [3]. These effects were confirmed by the measurement of effective vertical field and effective mobility as shown in Fig.4. Furthermore, as shown in Fig.5, a high frequency characteristic such as cut-off frequencies (f_t and f_{max}) was measured, and it ascertained that a conductance characteristic improved due to the mobility improvement.

To verify the circuit performance of depletion SOI-MOS, 1/8 frequency divider was evaluated with differential ED-MOS/SOI circuit as shown in Fig.6. The values of the threshold voltage of depletion, and zero-Vth MOSFETs are -0.168 and 0.01V. The dependence of the maximum operating frequency on the power dissipation power at each operating supply voltage both 0.15um and 0.25um SOI are shown in Fig.7. The maximum operating frequency of 0.15um ED-CMOS/SOI is about 10 GHz, and which is about 1.8 times lager than that of 0.25um ED-CMOS/SOI [1]. At a power dissipation of 1mW, the operating frequency 7.5GHz is achieved. Only the ED-CMOS/SOI circuit makes it possible to operate ultrahigh-speed frequency below 1V power supply.

Acknowledgements

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References

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[2] T.Ichimori, et al., Ext. Abs. on SSDM, pp.478, 200
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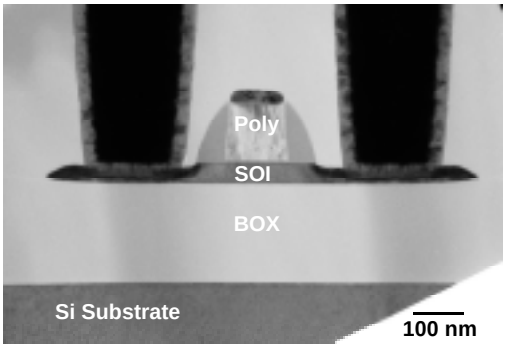

Fig.1A. Cross section TEM image of Gate Length 0.15um SOI MOSFET.

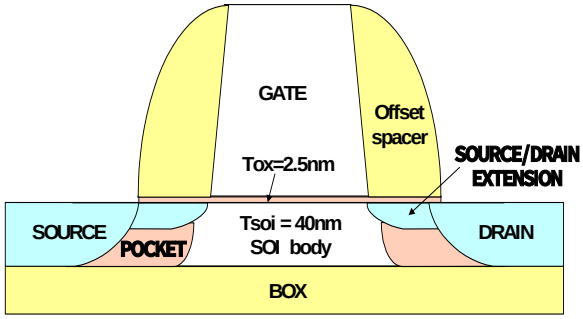

Fig.1B. Device Strucure corresponding to TEM image.

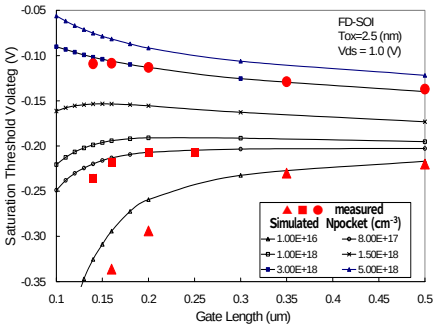

Fig.2A Measured (■ ▲ ●) and simulated (solid line) gate length dependence of the saturation threshold voltage with the various impurities concentration of the pocket region.

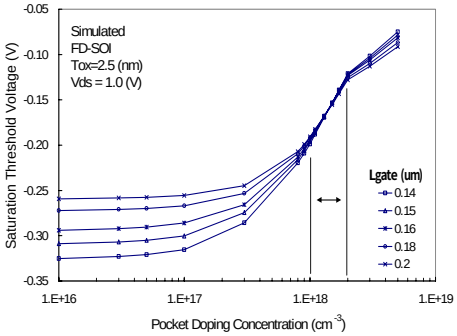

Fig.2B Simulated pocket doping concentration dependence of the saturation threshold voltage. The optimal pocket doping region is indicated by arrows.

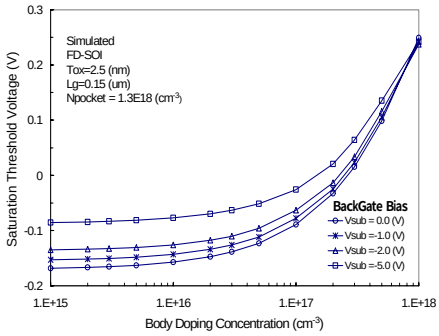

Fig.2C Simulated body doping concentration dependence of the saturation threshold voltage for the optimal pocket doping FD-SOI.

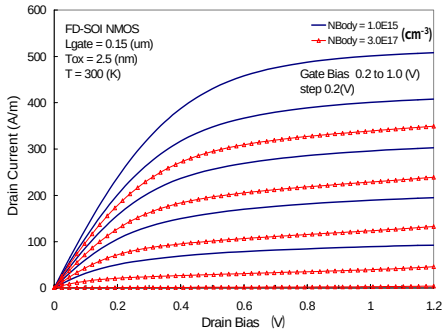

Fig.3 Comparison of the measured Id-Vd characteristics of undoped DMOS and enhancement type.

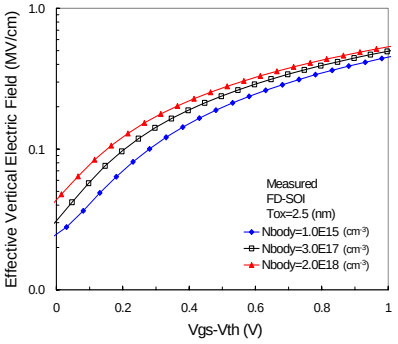

Fig.4A Measured gate bias dependence of the effective vertical electric field under various body doping condition.

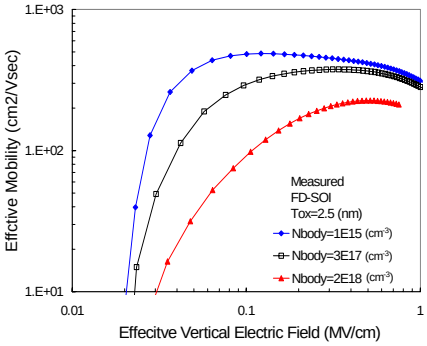

Fig.4B Measured effective vertical electric field dependence of the effective mobility under various body doping condition.

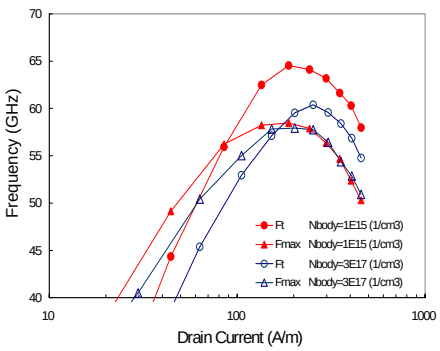

Fig.5. Measured high frequency characteristics (ft and fmax) both depletion and enhancement FD-SOI MOSFET.

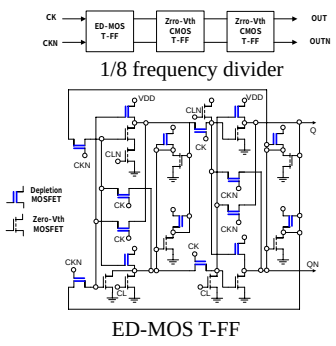

Fig.6. Differential ED-CMOS/SOI circuit scheme.

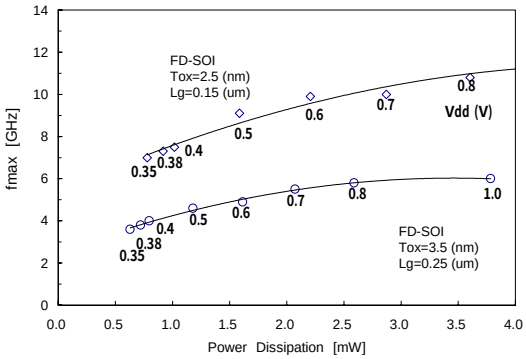

Fig.7. Maximum operating frequency vs. power dissipation for the ED-CMOS/SOI frequency divider.