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A 0.5-V Noise-Shaping A/D Converter Using Low-Threshold FD-SOI Transistors

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1. Introduction: LSI process technology is scaling down to under 0.1 um, and the supply voltages to LSIs are decreasing in proportional to the scale-down. In the near future, the supply voltage to analog circuits will be below 1 V. Therefore, a key technology for the next-generation of analog circuits is low-voltage operation of about 0.5 V. To demonstrate the possibility of lowering the supply voltage to less than 1 V, we fabricated a 0.5-V noise-shaping A/D converter using 0.35-um low-threshold FD-SOI CMOS process technology.

2. Merits using FD-SOI transistor for analog circuits:

Very low diffusion capacitance and low leakage current of fully depletion (FD) SOI transistor are beneficial for achieving low-supply- voltage analog circuits. Figure 1 (a) shows a simple push-pull amplifier circuit as an example of an analog circuit and Fig. 1 (b) is its equivalent circuit. The unity-gain frequency, which is a standard of performance, depends on the product of a first pole frequency and gain. The pole frequency can be improved by reducing the on-resistance (1/gdp, 1/gdn) and the parasitic capacitance (Cp, Cn). However, reducing the on-resistance decreases the gain, because the gain depends on gm/gd. Therefore, a low diffusion capacitance in SOI transistors is very useful for improving performance. Furthermore, lowering Vth improves the unity-gain frequency in under-1-V operation dramatically, as shown in Fig. 2. However, the leakage current increases exponentially with decreasing Vth, and comes to 10 % of the bias current in analog circuits in the case of a common bulk CMOS transistor with Vth of nearly 0.15 V, as shown Fig. 3. In this case, some trouble occurs, such as a narrowing of the dynamic-range and a slipping off from the bias point due to the I-R drop. So, the low-leakage-current characteristic of FD-SOI transistors is very well suited for low-voltage-supply analog circuits.

3. RC integration swing-suppression A/D converter:

We already reported a 1-V operation noise-shaping A/D converter using bulk CMOS [1], to which we applied a RC integration swing-suppression noise-shaping method. To apply low-Vth (0.15 V) FD-SOI CMOS transistors to it, we lowered the operation voltage by 1/2 (0.5 V). Figure 4 shows the swing-suppression A/D converter circuit. Integrators, which determine the accuracy, were constructed by a RC continuous-time integrator, because the characteristics of this passive device are not influenced by the supply voltage. A transistor that operates in the triode region is suitable for low-voltage operation, because it will operate even if Vsd is near zero. So, we applied the new latched comparator shown in Fig. 5. All transistors in it operate in the triode region. In this case, the body-floating effect of FD-SOI transistors does not influence the comparison accuracy. The amplifier (Fig. 6) is the only component whose transistors operate in the saturation region. The inverted amplifier fixes inputs to the virtual ground. Therefore, the narrow dynamic-range amplifier due to low voltage supply is possible to use.

4. Resolution: Figure 7 shows the layout of the test chip using the 0.35-um FD-SOI CMOS process. The Vth of transistors is ±0.15-V. The measured power spectrum is shown in Fig. 8. The noise floor is about –90 dB, and second and third distortions are about –80 dB. The measured S/N+THD is shown as a function of input level in Fig. 9, and the performance is summarized in Table 1. DRs of 78 (14-bit accuracy) and 59 dB (10-bit accuracy) at the bandwidths of 20 and 200 kHz are obtained. The power-consumption is 1.3 mW at a 0.5-V supply. The performance is good enough for the audio interface and digital communications interfaces up to 400 kbps.

5. Conclusion: We have described a 0.5-V operation noise-shaping A/D converter using low-threshold FD-SOI transistors. S/Ns of 78 (14-bit accuracy) and 59 dB (10-bit accuracy) at bandwidths of 20 and 200 kHz are obtained. These results show that analog circuits that are operated near 0.5 V can be built using FD-SOI CMOS transistors.

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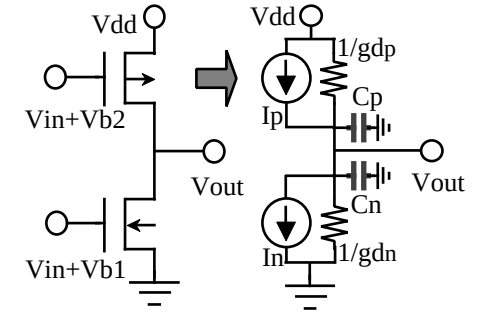
Reference [1] Y. Matsuya, K. Uchimura, A. Iwata and T. Kobayashi, "A 16-bit Oversampling Triple-Integration Noise Shaping." IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 921-929, Dec. 1987.



(1) Circuit structure (2) Equivalent circuit

Fig. 1 Push-pull amplifier structure

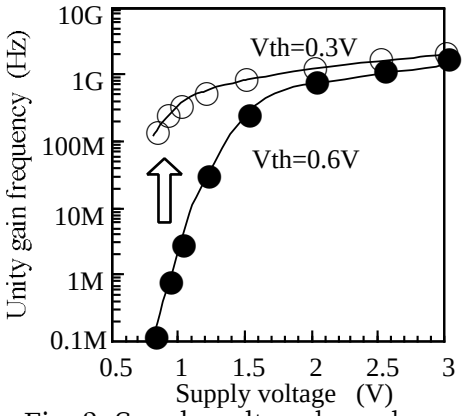


Fig. 2 Supply voltagedependence of unity gain frequeny

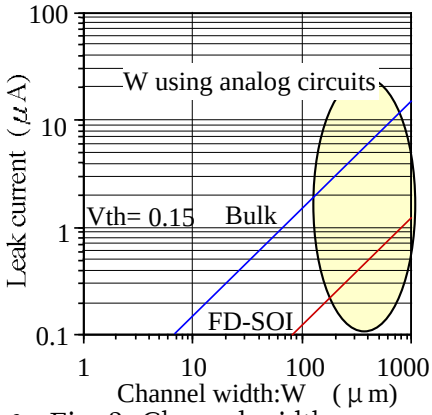


Fig. 3 Channel width dependence of leak current

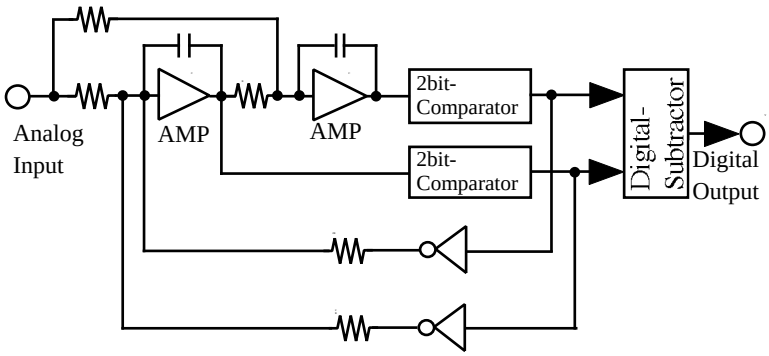


Fig. 4 A/D converter circuit

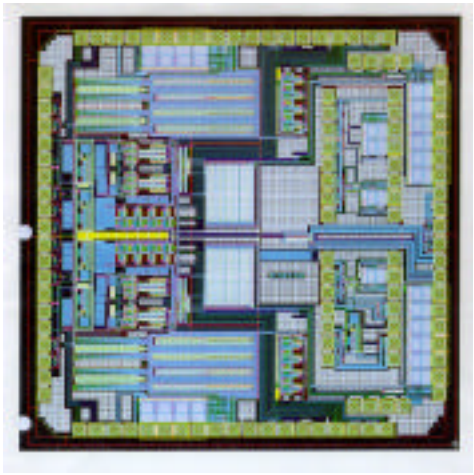


Fig. 7 Layout of A/D converter

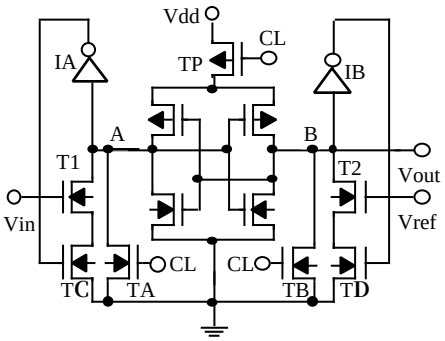


Fig. 5 Comparetor circuit

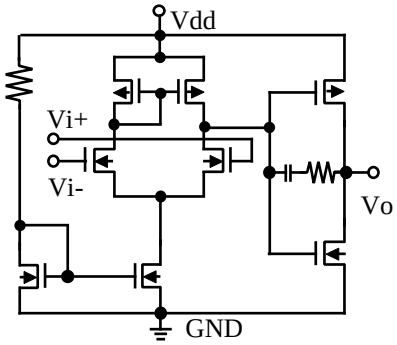


Fig. 6 Amplifier circuit

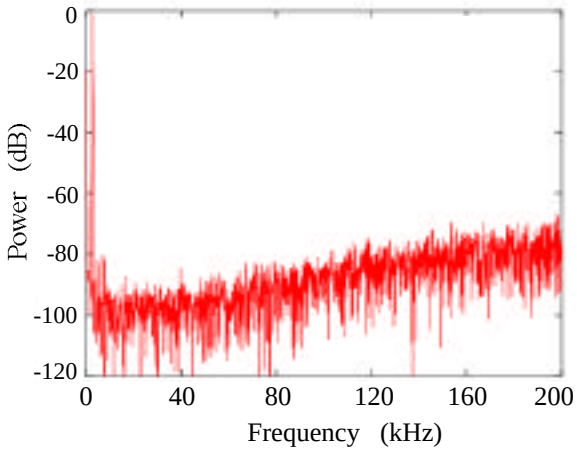


Fig. 8 Measured power spectrum

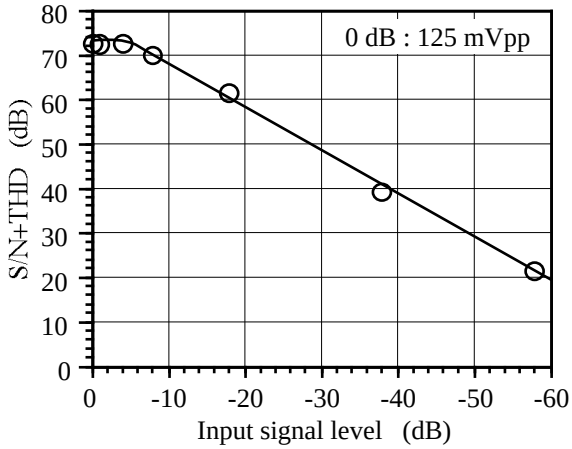


Fig. 9 Measured S/N+THD preformance

Table 1 Performance

Signal bandwidth	20 kHz	200 kHz
Resorution	14 bit	9 bit
S/N+THD	72 dB	55 dB
DR	78 dB	59 dB
Supply voltage	0.5 V	
Input dynamic range	125 mV(Vdd/4)	
Power consumption	1.3 mW	
Chip size	4 mm x 4 mm	