Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 46-47

C-1-1 (Invited)

Mobility in high-κ dielectric based field effect transistors

L-Å Ragnarsson[a],
W. Tsai[b], A. Kerber[c], P.J. Chen[d], E. Cartier[e], L. Pantisano[a], S. De Gendt[a], and M. Heyns[a]
[a]IMEC, [b]Intel Corp., [c]Infineon, [d]Texas Instruments, [e]IBM
c/o IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, E-mail: Lars-Ake.Ragnarsson@imec.be

1. Introduction

The integration of high-κ dielectrics into future CMOS technologies is currently under intense investigation. Several key integration challenges have been identified including charge trapping and reduced carrier mobility. Furthermore, electrical characterization difficulties of such materials have been addressed [1,2]. In this presentation, the focus is on the mobility extraction and issues related to it. Results from ultrathin high-κ stacks will also be discussed.

2. Experimental

Measurements

Mobility measurements are traditionally carried out using the split *C–V* technique [3]: i) the inversion capacitance is measured and integrated to determine the inversion charge; and ii) the static (DC) drain current (I_{DS}-V_{GS}) is measured in the linear region (low V_{DS}). From these two measurements the effective field and mobility can be calculated [3]. However, in devices which trap charge during the measurement this technique is not reliable. In an *n*FET, electron trapping leads to overestimated inversion charge and underestimated current. Hence, the calculated electron mobility is often underestimated and the effective field overestimated. For *p*FETs the charge trapping is considerably less of a problem [4].

To facilitate accurate measurements on such materials, non-standard techniques have to be employed. In this presentation, the inversion charge error is estimated from two alternative techniques: i) inversion charge pumping (ICP) [2] and ii) the Hall effect [5]. In ICP, the inversion charge is measured with charge pumping on a long device (20-100 μm). From this measurement, both the inversion and trapped charge are measured. With the trapped charge measured on a short device (1 μm), the actual inversion charge can be calculated. The I_{DS}-V_{GS} is measured using a similar technique at the same frequency as the ICP. The main advantage of this technique as compared to the split *C-V* method is the ability to measure at high sweep rates and thus to minimize the amount of charge that is trapped during the measurement.

With the Hall effect, the true inversion charge can be measured directly from the Hall voltage which builds up across the channel when a perpendicular magnetic field is applied [6].

Here it should be pointed out that although it is possible to correctly measure the mobility in devices which trap charge, this mobility is an intrinsic value. Naturally, any device based on such a material will be inferior to a device with a trap-free one. There might still be room for improvement, if the poor characteristics of the dielectric is extrinsic to the material and therefore can be improved under optimum growth/anneal conditions.

In addition to the mobility, transconductance (g_m) is often used as an indicator of the device/dielectric performance. The g_m values are significantly easier to measure correctly, but does not only depend on the mobility, but also on the device geometry and inversion capacitance. A low mobility can thus be compensated for with a higher inversion capacitance achieved e.g. by switching from poly-Si to a metal gate. Hence, the g_{mpeak} values should be used as an indication of the overall performance of a gate stack. To simplify the comparisons, g_m curves and peak values are here normalized with the width to length ratio and the drain bias.

For devices with extremely scaled dielectric stacks, leakage current problems make accurate mobility assessments even more problematic. Furthermore, the ICP technique cannot be employed if gate-leakage is non-negligible. Fortunately, our studies on V_T instability show that charging is less of a problem in ultrathin dielectric stacks, simply because there is less high-κ and therefore less traps to charge. The results presented for such scaled stacks are therefore based on the split *C-V* method. If possible, long devices (L=10 μm) were used to measure the mobility. In cases where the leakage current was too large so that shorter devices were needed, care was taken to estimate the series resistance and compensate for it.

Devices

Two approaches towards scaling was explored in this study: i) the use of a scaled interfacial oxide and ii) gradual decrease of the number of ALCVD™ [7] cycles deposited. In the case of poly-Si gated devices, low cycle counts result in yield problems. For these devices, scaling was achieved by interfacial layer thinning. The poly-Si gated *n*FETs were manufactured using a standard self-aligned process [8]. For TiN-gated devices, samples with 30-100 cycles of HfO_2 were deposited on top of a scaled interfacial oxide. The metal gate devices (*p* and *n*FETs) are from a gate last process with sputtered TiN.

Hall mobility measurements were carried out on specially designed transistors with tabs connected to the channel [6].

3. Results and Discussion

Fig. 1 shows the errors in peak effective mobility as estimated from the ICP and Hall measurement techniques. The correction ranges from 8 to 37% but the corrected values are in all cases considerably lower than the

corresponding SiO_2 values showing that additional scattering processes are present. Furthermore, the Hall samples reveal that two samples with apparently very different mobility can in reality have very similar mobility but trap charge to a different degree.

Fig. 2 shows a comparison of the electron mobility for poly-Si gated devices with a scaled interfacial oxide. The mobility is reduced for the thinner interfacial oxide.

Fig. 3 shows a series of mobility curves measured on TiN gated HfO_2. The electron mobility is degraded severely as compared to the universal mobility and the deviation increases for the thinner stacks. Therefore, instead of the expected increase in $g_{m,peak}$ with lower EOT, g_m decreases below an EOT of ~10 Å (Fig. 4). In contrast, the hole mobility is close to the universal curve except at high fields and independent of thickness down to ~40 cycles of HfO_2 (EOT=8.5 Å).

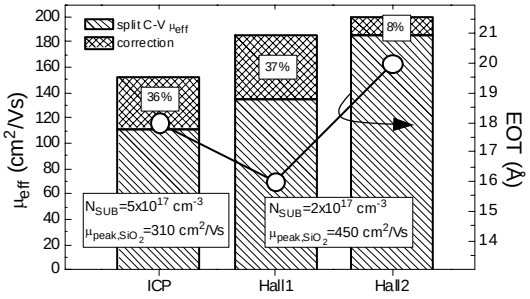

Fig. 1 The effective mobility corrections for poly-Si/HfO_2 devices from the ICP ad Hall effect methods. Also shown is the corresponding EOT. Note the different doping levels.

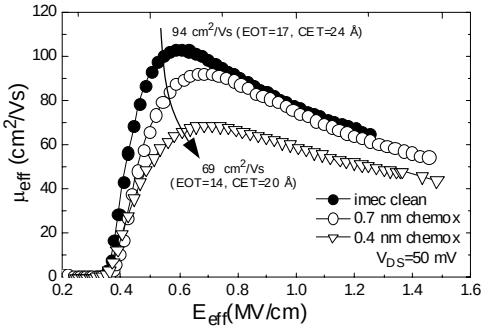

Fig. 2 The effective mobility for poly-Si/HfO_2(80 cycles) nFETs with a scaled interfacial oxide in comparison to an imec clean interface (~1 nm).

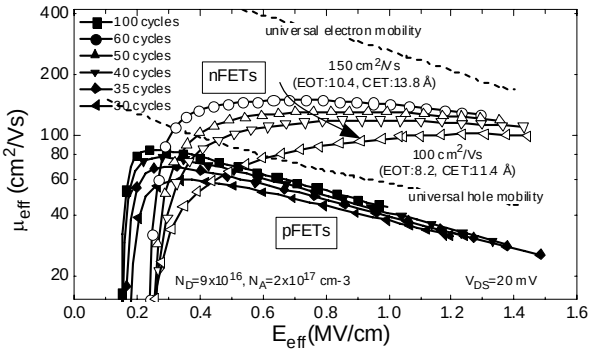

Fig. 3 The effective electron and hole mobility for TiN/HfO_2 *n*- and *p*-FETs with a scaled interfacial oxide (~0.4 nm).

Hence, for the *p*FETs, the reduced EOT results in increased $g_{m,peak}$ values all the way down to 8 Å. In Fig. 5 the mobility is shown as a function of the interfacial oxide thickness (t_{int}). The mobility for all *n*FET devices shown here scale with t_{int}, higher mobility with thicker interfacial oxides. Also, TiN devices have considerably higher mobility than the poly-Si FETs at equal t_{int}. Also shown in Fig. 5 is the measured and ICP corrected mobility from Fig. 1.

4. Conclusions

Different inversion charge measurement techniques are employed to account for charging effects in high-κ dielectrics – in this case HfO_2. The corrected mobility is shown to be 10-40% higher than the value measured with conventional techniques. We further show device results from TiN gated devices with EOT as low as 7.5 Å. As far down as 8 Å, the transconductance of the *p*FETs is improved, whereas for *n*FETs, a degraded electron mobility for the thinner stacks counteracts the benefits from the EOT scaling, resulting in a loss in overall transistor performance.

References

[1] L.-Å. Ragnarsson, et al, Proc of IEEE SISC, Washington D.C. (2001).
[2] A. Kerber et al, Proc of VLSI Technology, Kyoto, Japan (2003).
[3] S.-I. Takagi and M. Takayanagi, Jpn. J. Appl. Phys. **41**, 2348 (2002).
[4] A. Kerber, E. Cartier, L. Pantisano et al, Proc. of IRPS, p. 41 (2003).
[5] O. Lindberg, Proc. of the I.R.E. p.1414 (1952). K. B. Joelsson, Y. Fu, W.-X. Ni, and G. V. Hansson, J. Appl. Phys., **81,** 1264 (1997).
[6] The Hall measurements were carried out at IBM T.J. Watson Research Center, Yorktown Heights, (submitted to EDL).
[7] ALCVD is a trademark of ASM International, Bilthoven, The Netherlands.
[8] S. Kubicek, et al, *to be presented* at ESSDERC, Portugal (2003).

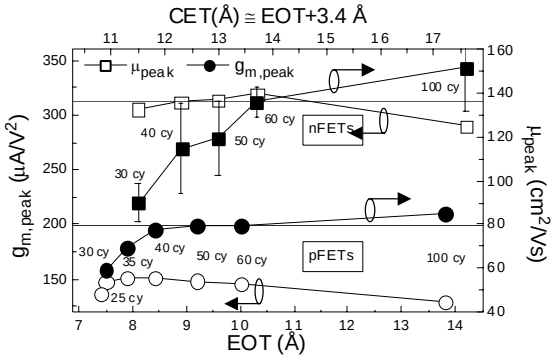

Fig. 4 $g_{m,peak}$ and μ_{peak} vs EOT for poly-Si gated *n*FETs and TiN gated *n*- and *p*-FETs.

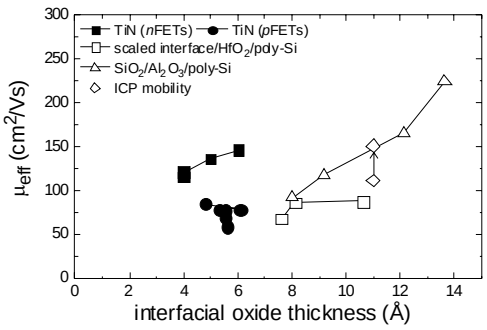

Fig. 5 The peak effective mobility vs. the interfacial oxide thickness for poly-Si and TiN/HfO_2 devices. Also shown are Al_2O_3/poly-Si values and the ICP values from Fig. 1.