

## Ultra-thin (EOT < 1.0nm) Amorphous HfSiON Gate Insulator with High Hf Concentration for High-performance Logic Applications

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### I. Introduction

N incorporated Hf silicate (HfSiON) is expected to be applied as an alternative gate insulator to silicon dioxide (SiO<sub>2</sub>) for next-generation LSIs.<sup>1,2</sup> This is because N in HfSiON can prevent the phase separation and micro-crystallization which may cause a decrease in permittivity and an increase in the propagation gate delay of CMOS circuits.<sup>3,4</sup> The suppression of boron penetration can also be realized in this material.<sup>2,5</sup> For its application to high-performance CMOS logic devices, however, the equivalent oxide thickness (EOT) of HfSiON must be scaled to less than 1.0nm, keeping the leakage current level low.<sup>6</sup>

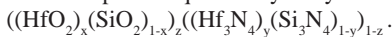
In this study, we investigated the properties of HfSiON films with high Hf concentrations ([Hf]/([Hf]+[Si]):60~80%) intensively. We found that HfSiON films with [Hf]/([Hf]+[Si]) of 80% and [N] of more than 20at.% kept amorphous phase when high-temperature annealing was performed with a poly-Si cap. It was also found that higher Hf concentration led to higher dielectric constant without severe degradation of leakage current of the film in this composition range. As a result, EOT scaling to <1.0nm with 10<sup>4</sup> times lower leakage current than that of SiO<sub>2</sub> was successfully demonstrated by ultra-thin HfSiON/interfacial-layer stacked insulators.

### II. Experiment

HfSiON films were deposited on p-Si(100) wafer by co-sputtering of Hf and Si targets. The atomic compositions were controlled by the flow rates of gasses (Ar/O<sub>2</sub>/N<sub>2</sub>) and by the sputtering power of targets. The bonding states, compositions, and structural information were analyzed by X-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectrometry (RBS), cross-sectional transmission electron microscopy (XTEM) and X-ray diffractometry (XRD). To investigate the electric properties, MIS capacitors (n<sup>+</sup>-poly Si gate electrode /HfSiON film/p-Si(100) substrate) were fabricated. High-temperature annealing such as 1000°C RTA in N<sub>2</sub> or spike annealing at 1065°C was performed to activate the impurity in the poly Si gate electrode. In the final process, forming gas annealing at 450°C was carried out.

### III. Results and Discussion

First, we show the bonding states of HfSiON films. In Figs. 1(a) and 1(b), Si2p and Hf4f peaks from the film ([Hf]/([Hf]+[Si]): 60%, physical thickness: ~100nm) are represented, respectively. These peaks shift to lower binding energy with increasing [N]. This result indicates that Si-O and Hf-O bonds decrease and Si-N and Hf-N bonds increase as [N] increases. From Hf4f spectra, no peak of Hf-Hf and Hf-Si bonds was observed. The relation between [N] and [O] of HfSiON with various compositions by RBS is plotted in Fig. 2. All data points fall almost on a straight line, corresponding to the tie line of ternary composition diagram for stoichiometric SiON. On the analogy of SiON,<sup>7</sup> HfSiON films fabricated in this study are regarded as a pseudo-quaternary alloy:



This alloy model is consistent with the result for bonding states by XPS (Fig. 1). Since no metallic component like Hf-silicide is included, it is expected that this HfSiON film acts as a good insulator even at high Hf composition.

Next, we investigated the thermal stability of HfSiON films. Figures 3 (a) and 3 (b) show the XTEM images of HfSiON films with-

out and with poly-Si cap, annealed at 1000°C for 30sec in N<sub>2</sub>. In the former case HfSiON is fully crystallized (Fig. 3 (a)), whereas in the later case HfSiON is not crystallized (Fig. 3 (b)). Since it was revealed by XPS that Hf-O signal from the HfSiON film increases after the annealing without the poly Si layer (data not shown), we conclude that N decrease after the annealing shown in Fig. 4 is caused by residual O<sub>2</sub> in N<sub>2</sub> ambient; N bonded to Hf in the film is easily replaced by O and diffused out of the film. This model is quite reasonable because higher Hf causes greater N-outdiffusion after the annealing without poly Si (Fig. 4). The improvement of the thermal stability of the HfSiON film capped with poly Si can be explained in terms of preservation of [N] in the films after the annealing. Figure 4 also shows that the same amount of [N] remained in the film with the poly Si cap layer after the annealing. XRD analysis of the films with [Hf]/([Hf]+[Si]) of 80% was performed as shown in Fig. 5. Peaks of both HfO<sub>2</sub> and Si (from poly Si cap and the substrate) appeared in the film without nitrogen after spike annealing at 1065°C. On the contrary, peaks of HfO<sub>2</sub> crystals were not observed in HfSiON with [N] of 20at.%, indicating that the film kept amorphous phase.

We show here the electric properties of HfSiON films. The capacitance-voltage (C-V) characteristics of the thin films are represented in Fig. 6. Although these physical thicknesses are almost the same, the HfSiON film with higher [Hf]/([Hf]+[Si]) and [N] gives larger capacitance, indicating higher dielectric constant. This means that increasing Hf and N concentrations effectively enhances dielectric constant. Figure 7 shows a cross section of the poly Si/HfSiON/Si structure for EOT of less than 1.0nm. It was confirmed that the Hf concentration in the dielectric is depleted near the substrate interface, leading to well-behaved C-V curves of the MIS structure (Fig. 6). The average dielectric constant of the stacked insulator was estimated to be 14, meaning that the HfSiON layer itself has much higher dielectric constant than 14. Figure 8 shows Jg-Vg characteristics of HfSiON films with [Hf]/([Hf]+[Si]) of 60% and 80%. The difference in leakage current between specimens at the same gate voltage is kept within one order or less, although [N] of the film is widely changed from 15 to 50at.%. The relation between EOT and Jg of HfSiON films with high Hf concentration is represented in Fig. 9. The trend for SiO<sub>2</sub> is also depicted here. As shown in Fig. 9, EOTs of less than 1.0nm were successfully demonstrated with gate leakage current 10<sup>4</sup> times lower than that of SiO<sub>2</sub>. Leakage currents of our HfSiON films with high Hf concentrations are about two orders of magnitude lower than those of previously reported results.<sup>5</sup> To our knowledge, this is the largest reduction of the leakage current relative to those of SiO<sub>2</sub> for thermally stable amorphous high-k film with EOT of less than 1.0nm.

### IV. Conclusions

We studied the structural and electric properties of HfSiON films with high Hf concentration. The films fabricated in this study keep amorphous phase even after annealing at high temperature of 1065°C, and show excellent electric property such as Jg < 1A/cm<sup>2</sup> at Vfb-1(V) and EOT < 1.0nm.

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## References

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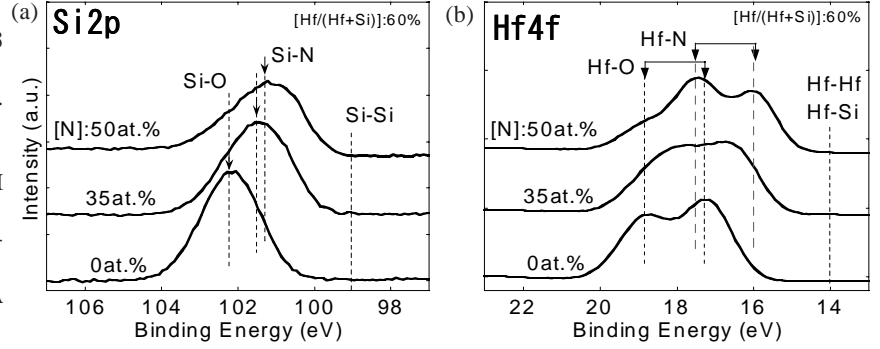


Fig.1: XPS data of (a) Si2p and (b) Hf4f from HfSiON films with [Hf]/([Hf+Si]) of 60%. [N] in HfSiON films are 0, 35 and 50at.%, respectively.

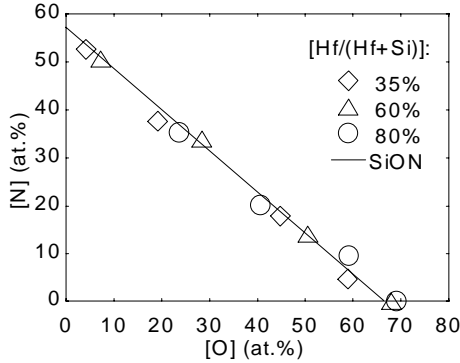


Fig.2: Relation between [O] and [N] of HfSiON films with various atomic compositions. The line for stoichiometric SiON is also shown.

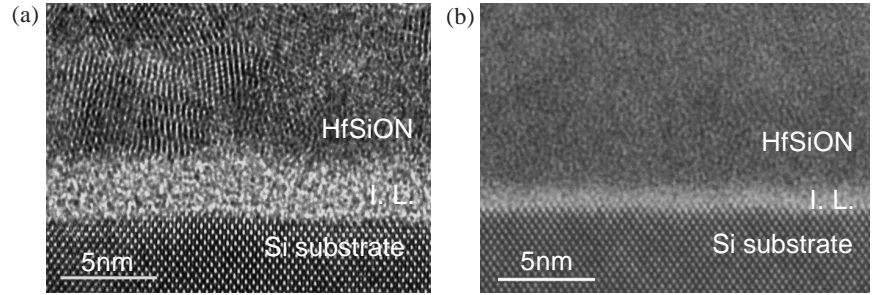


Fig.3: XTEM images of HfSiON (a) without and (b) with poly Si cap after annealing. Before annealing, [N] and [Hf]/([Hf+Si]) were 38at.% and 55% in the former case, while [N] and [Hf]/([Hf+Si]) were 33at.% and 60% in the later case.

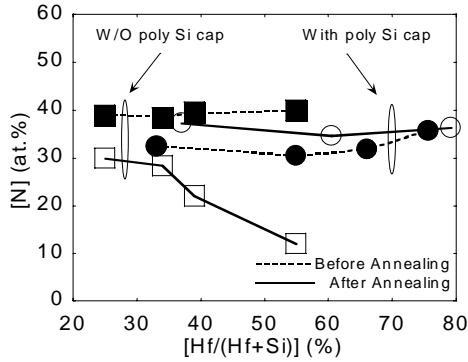


Fig.4: Change of atomic compositions in HfSiON with and without poly Si before and after annealing. Dotted and solid lines refer to the case before and after annealing, respectively.

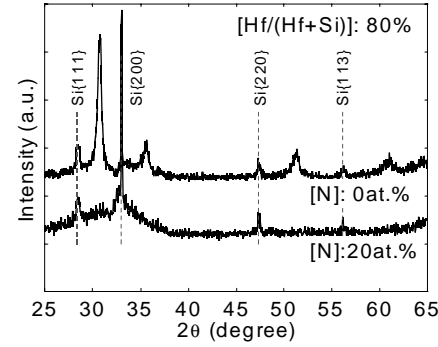


Fig.5: XRD patterns from HfSiO and HfSiON with 20at.% of [N]. [Hf]/([Hf+Si]) is 80%. Spike anneal was carried out at 1065°C. Si peaks are from poly Si cap and the substrate.

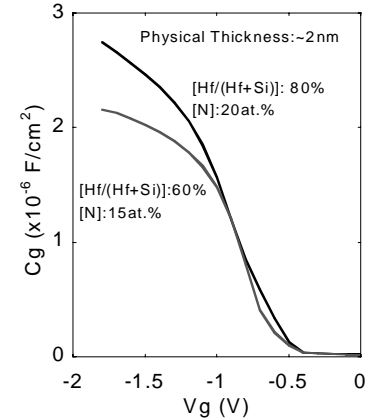


Fig.6: CV curves of two kinds of HfSiON thin films. Their composition of [Hf]/([Hf+Si]) are 60 and 80%, and those of [N] are 15 and 20at.%, respectively.

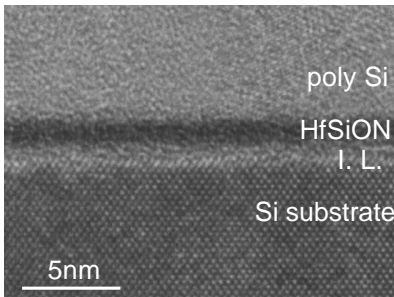


Fig.7: XTEM image of the ultra thin gate stack HfSiON with [Hf]/([Hf+Si]) of 80% and [N] of 20at.% after 1065°C spike annealing.

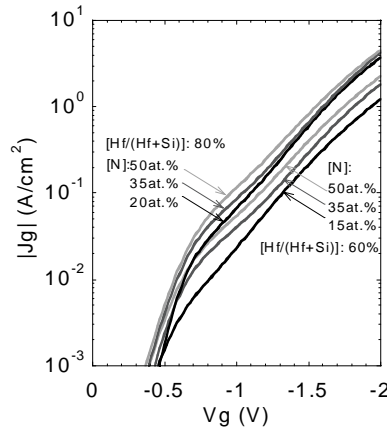


Fig.8: Relation between leakage current and gate voltage of HfSiON with [Hf]/([Hf+Si]) of 60% and 80%.

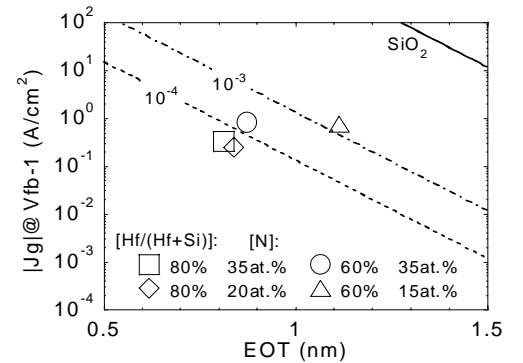


Fig.9: Relation between EOT and  $J_g$  of HfSiON thin films. The trend line of  $\text{SiO}_2$  is also depicted.