Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 58-59

C-2-2

Controlled Nitrogen Incorporation into $HfAlO_x$ by Layer-by-Layer Deposition and Annealing (LL-D&A) Process and Its Impact on Electrical Properties of MOSCAPs and nMOSFETs

K. Tominaga[1], K. Iwamoto[1], H. Hisamatsu[1], T. Yasuda[2], H. Ota[2], N. Yasuda[1], T. Nabatame[1], and A. Toriumi[2, 3]

[1]MIRAI-ASET, AIST Tsukuba West 7, 16-1, Onogawa, Tsukuba, Ibaragi 305-8569, Japan
Phone: +81-29-849-1549 FAX: +81-29-849-1529, E-mail: koji.tominaga@mirai.aist.go.jp
[2]MIRAI-ASRC, AIST Tsukuba, Japan, [3]Department of Materials Science, the University of Tokyo, Japan

1. Introduction

Continuing down-scaling of LSI requires alternative materials with high dielectric constants (high-k), since the gate leakage current becomes unacceptably large when thickness of conventional gate oxide or oxynitride is reduced to <1nm. Possible candidates of high-k gate dielectrics include HfON [1], $HfAlO_x$ [2], and HfAlON [3]. Among various growth techniques, atomic layer deposition (ALD) is expected to be suited for ultra-thin high-k oxide formation. We have proposed a new processing concept of layer-by-layer deposition and annealing (LL-D&A) which combines ALD with rapid thermal annealing (RTA) in a single processing system [4]. In the LL-D&A, a sequence of given cycles of ALD and subsequent RTA is repeated to obtain a target films thickness. As shown in our previous report [4], the inserted RTA treatment efficiently removes residual carbon impurities from the deposited high-k films.

In this paper, we focus on another unique feature of the LL-D&A process, namely, controlled nitrogen incorporation into the high-k oxides. By performing the inserted RTA in NH_3 ambient, we can control the depth profile of nitrogen in the gate stack. We have fabricated MOSCAPs and nMOSFETs with HfAlON dielectrics using this technique, and investigated the impact of nitrogen incorporation on the electrical properties of MOS capacitors and nMOSFETs.

2. Experimental

P-type Si(100) wafers were thermally nitrided in NH_3 ambient to a thickness of 0.4nm prior to high-k film deposition. In this study, HfAlON formation by LL-D&A was carried out in five steps as shown in **Fig. 1**. In the first step, an about 0.8nm-thick $HfAlO_x$ (Hf:60at.%) layer was deposited by ALD using $Al(CH_3)_3$, $Hf[N(CH_3)_2]_4$ and H_2O at 250°C. This layer was subjected to *in situ* RTA at 650°C for 30s in either NH_3 or O_2 (130Pa). Each of the second, third and fourth steps consist of ALD growth by about 0.8nm and subsequent RTA in O_2. In the fifth step, the final ALD growth was followed by RTA in the same gas as used in the first step. In this paper, D&A(NH_3/O_2×3/NH_3) denotes the case where RTA treatments in the first and fifth steps were performed in NH_3, and the other three steps in O_2, while D&A(O_2) denotes the case where they in all steps were done in O_2.

The reason for setting the RTA temperature at 650°C is as follows. **Figure 2** shows Si_{2p} XPS spectra for the $HfAlO_x$/SiN/Si structures fabricated by the D&A(O_2) process with three different RTA temperatures. The D&A(O_2) process induces oxidation of the SiN layer and Si substrate, and the interfacial SiON layer becomes thicker with increasing the RTA temperature. In the case of 650°C process, the interfacial SiO_2 layer thickness is estimated to be 0.65nm, which is marginally acceptable for the purpose of EOT scaling. On the other hand, RTA at temperatures lower than 650°C was not effective for efficiently desorbing residual impurities [4].

The poly-Si gate nMOSFETs were fabricated by the conventional gate stack processes.

3. Results and Discussion

Figure 3 shows a SIMS profile for nitrogen in a $HfAlO_x$/HfAlON/SiON/Si stack structure. The $HfAlO_x$ layer was capped by ALD after HfAlON formation by D&A(NH_3/O_2×3/NH_3). This indicates that RTA in NH_3 indeed introduces nitrogen into $HfAlO_x$. In principle, we can control the nitrogen concentration and its depth profile by adjusting conditions and insertion step of the NH_3 annealing during ALD process.

Figure 4 shows a cross-sectional TEM image of a poly-Si/HfAlON/SiON/Si stack that was annealed for the source/drain activation at 850°C for 10min. Note that the HfAlON film maintains an amorphous structure. Thicknesses of the HfAlON film and interfacial layers are about 3.9nm and 0.6nm, respectively.

C-V characteristics for MOSCAPs with n+ poly-Si gate are shown in **Fig. 5**, where results for three different deposition processes are compared. These are D&A(NH_3/O_2×3/NH_3), D&A(O_2), and conventional ALD followed by PDA. The parameters extracted from the C-V characteristics are summarized in **Table 1**. The D&A(NH_3/O_2×3/NH_3) and D&A(O_2) processes improve the flat-band voltage hysteresis, V_{hys}, as compared to the ALD. Furthermore, D&A(NH_3/O_2×3/NH_3) process can suppress the increase of EOT compared to that of D&A(O_2). In fact, by using XPS, we obtained that the interfacial layer for $HfAlO_x$/SiN prepared by D&A(O_2) was thicker than those by D&A(NH_3/O_2×3/NH_3) or ALD process.

Figure 6 shows the relationship between EOT and leakage current density. The samples prepared by three different deposition processes show the leakage current reduction by about 4 orders of magnitude as compared to the thermally grown SiO_2.

Finally, **Figure 7** shows the electron mobility in nMOSFETs. The inversion layer mobility of nMOSFETs with the D&A($NH_3/O_2\times3/NH_3$) and D&A(O_2) processes are significantly higher than that for conventional ALD, demonstrating the effectiveness of the LL-D&A processing for improving the gate stack properties. The peak mobility for the D&A($NH_3/O_2\times3/NH_3$) is 240cm^2/Vs which is slightly higher than that for D&A(O_2). We think that this improvement may come from the decrease of Coulombic scattering centers. As summarized in Table 1, the flat-band voltage shift, δV_{FB} is smallest for the D&A($NH_3/O_2\times3/NH_3$) process, indicating that effective density of the fixed charges is decreased by this process.

4. Conclusion

We have proposed and demonstrated a new process for high-k dielectrics formation, namely, layer-by-layer deposition and annealing (LL-D&A) associated with NH_3 annealing. This paper has addressed its unique feature that the nitrogen profile in the high-k layers can be controlled by inserting RTA treatment in NH_3 ambient. nMOSFETs with HfAlON gate dielectrics have shown an improved peak mobility of 240cm^2/Vs at EOT of 1.29nm.

Acknowledgements

This work was supported by NEDO.

References

[1] C. H. Choi et al., IEDM Tech. Dig., p857 (2002).
[2] G. D. Wilk et al., VLSI Symp. Tech. Dig., p89 (2001).
[3] H. S. Jung et al., IEDM Tech. Dig., p853 (2002).
[4] K. Iwamoto et al., Abstract, No.918, in 203rd ECS Meeting, Paris (2003).

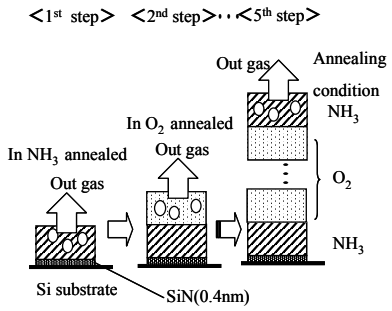

Fig.1 HfAlON formation by LL-D&A process. The LL-D&A process can control the nitrogen incorporation in HfAlON by annealing in NH_3 or O_2 ambient.

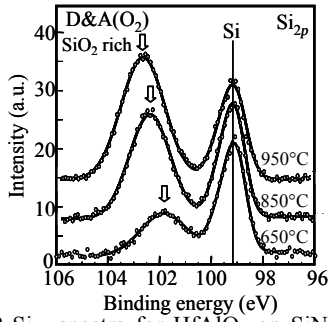

Fig.2 Si_{2p} spectra for $HfAlO_x$ on SiN/Si fabricated by D&A(O_2) process with three different annealing temperatures. As annealing temperature increases, the interfacial SiO_2 layer becomes thicker.

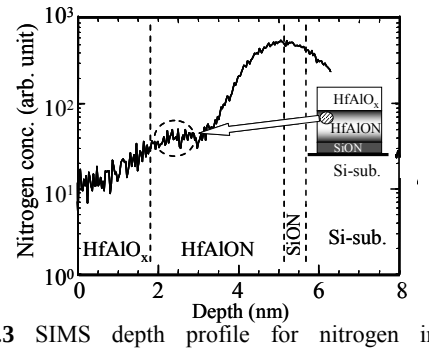

Fig.3 SIMS depth profile for nitrogen in $HfAlO_x$/HfAlON/SiON/Si stack structure. Extent of nitrogen incorporation and its location are controlled by adjusting the condition and insertion step of the NH_3 annealing.

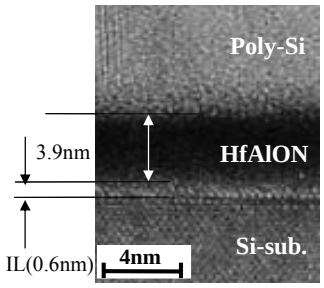

Fig.4 TEM cross-sectional image of poly-Si/HfAlON/SiON/Si gate stack structure. No crystalline structure is observed in HfAlON films.

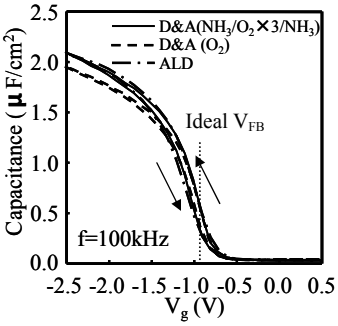

Fig.5 C-V curves for MOSCAPs with poly-Si gate. V_{hys} of D&A(O_2) and D&A($NH_3/O_2\times3/NH_3$) processes are improved compared to that of ALD.

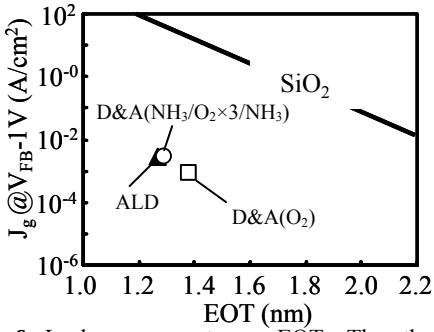

Fig.6 Leakage current vs. EOT. The three deposition processes show the leakage current reduction by about 4 orders of magnitude as compared to thermally grown SiO_2.

Table 1. Typical properties of MOSCAPs and nMOSFETs.

	ALD	D&A(O_2)	D&A ($NH_3/O_2\times3/NH_3$)
EOT (nm)	1.27	1.38	1.29
δV_{FB} (V)	0.18	0.18	0.15
V_{hys}(mV)	-90	-46	-63
Peak mobility (cm^2/Vs)	182	210	240

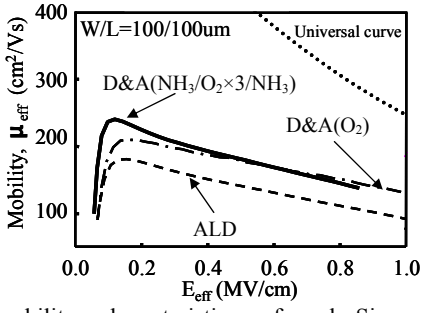

Fig.7 Electron mobility characteristics of poly-Si gate nMOSFETs. The peak mobility for D&A($NH_3/O_2\times3/NH_3$) is slightly higher than that of D&A(O_2). The improvement may come from the decrease of Coulombic scattering centers.