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Reliability characteristics of an HfO_2/SiO_2 stack gate dielectric annealed in a deuterium ambient

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1. Introduction

Due to the excess direct tunneling current and reliability limitations of Ultrathin SiO_2, the development of a high-k gate dielectric is necessary in achieving an effective oxide thickness of less than 1.5nm.[1] One of the major problems in using a High-K gate dielectric is its thickness independent low weibull slope $\beta(\approx 1\text{-}2)$ values. This low weibull slope β values in a high-K oxide are explained by extrinsic factors such as process induced defects. [2,3] In this presentation, we report on the improved reliability characteristics of HfO_2/SiO_2 stack gate dielectrics annealed in a D_2 ambient. The excellent reliability characteristics of deuterium annealed sample can be explained by the heavier mass effect.[4]

2. Experimentals

After the standard cleaning of a p-type silicon wafer, an approximately 1-nm thick layer of silicon dioxide(SiO_2) on 8-inch p-type silicon wafer was grown by the rapid thermal processing (RTP) in a pure O_2 ambient. These samples were transferred to an atomic layer deposition (ALD) system where a 12-nm thick Hafnium oxide(HfO_2) layer was deposited. MOS capacitors with 100nm-thick platinum gate(Pt) electrode were fabricated using a conventional photolithography process. After MOS capacitor fabrication, post metalization annealing(PMA) was performed at 450°C for 30 min in forming gas(4% H_2). For comparison, D_2 annealing was also performed at 450°C for 30min. The deuterium annealed sample contained deuterium, which was confirmed by time of flight - secondary ion mass spectroscopy (TOF-SIMS) using an 8kV Cs^+ primary ion beam.

3. Results & Discussion

Fig. 1 and 2 show capacitance versus gate voltage (C-V) and current versus gate voltage (I-V) for a MOS capacitor with a HfO_2(12nm)/SiO_2(1nm) stack film. The dispersion at various frequencies and hysteresis characteristics were negligible for both samples. Considering the identical I-V and C-V characteristics of both samples, we are able to confirm that the post metalization annealing in a D_2 ambient has no effect on the effective oxide thickness or the barrier height. To evaluate the charge trapping characteristics in the bulk oxide, flatband voltage shift (ΔV_{fb}) was monitored under a stress gate bias of –5V. Fig. 3 shows net-trapped charge density ($C_{ox} \times \Delta V_{fb}$) versus stress time for both samples. Both samples show a negative flatband voltage shift, indicating a net positive charge generation in the oxide bulk. This positive charge trap can be explained by hydrogen-release at the HfO_2 and SiO_2 interfaces.[5] Fig.4 shows the typical breakdown behavior of HfO_2(12nm)/SiO_2(1nm) stack, reduced soft breakdown characteristics are shown in deuterium annealed sample. Because of the heavy mass of deuterium, sample annealed in a D_2 ambient show less charge trapping characteristics and reduced soft breakdown characteristics. The generation of interface state density(ΔD_{it}) was monitored by a conductance method as shown in Fig.6.[6] Both samples were stressed at a gate bias of -5V. As shown in Fig.5 (a) and (b), the deuterium annealed sample shows a lower conductance loss peak(G_p/ω) under the same stress conditions. We confirmed that the D_2 annealed sample shows significantly less interface trap generation under an electrical stress. The reduced charge trapping and interface trap generation under the same electrical stress can be attributed to the large deuterium kinetic isotope effect.[4] Fig. 7 shows a weibull plot of time-to-breakdown (t_{BD}) at a stress bias of -5.8V. Table 1 shows the weibull slope (β) and time-to-breakdown (t_{BD} @ 63%) for various stress bias conditions. From the table, the weibull slope for the deuterium annealed sample is approximately 80% higher than that of the control sample. The improvement in the weibull slope for the deuterium annealed sample can be explained by a decrease in hydrogen-induced defects and neutral traps.[5] We estimated the time-to-breakdown(t_{BD}) as a function of the gate voltage as shown in Fig.8. The solid lines correspond to 63% failure values, as measured at an area of $9\text{x}10^{-6}\text{cm}^2$. In addition, the dashed lines estimate the t_{BD} for a device area of 0.01% and a cumulative failure probability of 0.01%. Due to the higher weibull slope, the deuterium annealed sample shows a significant improvement in device lifetime and operating bias voltage.

4. Summary

The effect of D_2 post-metal annealing on the reliability characteristics of HfO_2/SiO_2 stack films was investigated. Compared with a forming gas annealed sample, the HfO_2/SiO_2 stack film that was annealed in a D_2 ambient exhibit excellent reliability characteristics such as less charge trapping, less generation of interface states density, and improved weibull slopes. By employing deuterium annealing, it is possible to the operating bias up to 0.4V on 0.1cm^2 and 0.01% without any degrading device reliability. This improvement can be attributed to a large deuterium kinetic isotope effect.

Acknowledgments
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References

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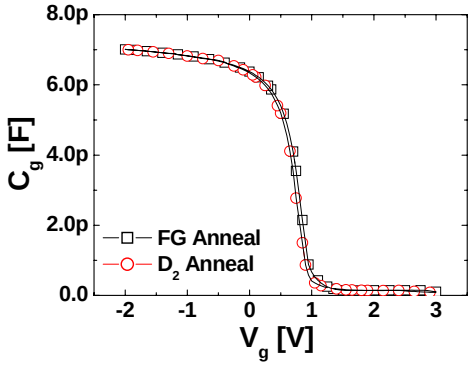

Fig.1 dentical Capacitance Vs. Voltage characteristic

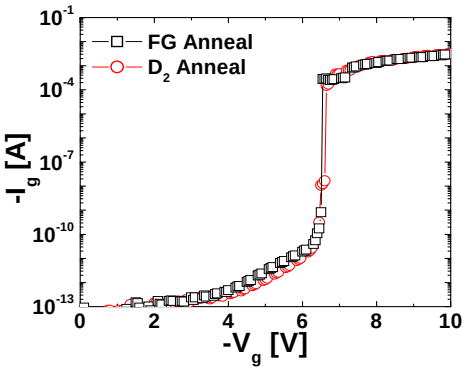

Fig.2 Leakage current Vs. gate voltage characteristic

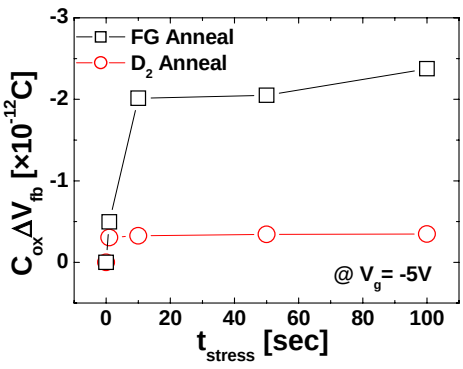

Fig.3 Net-trapped charge density ($C_{ox}\times\Delta V_{fb}$) characteristics varying with stress time.

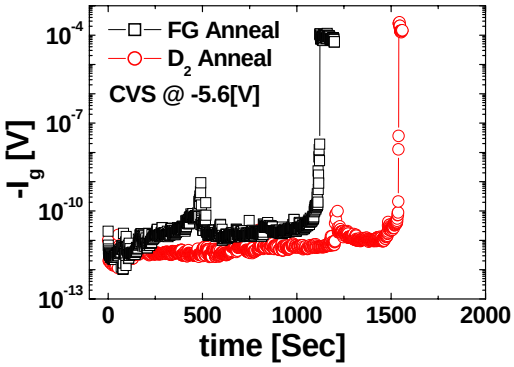

Fig. 4 Typical breakdown characteristics under the constant voltage stress. Reduced soft breakdown behavior is shown in D_2 annealed sample.

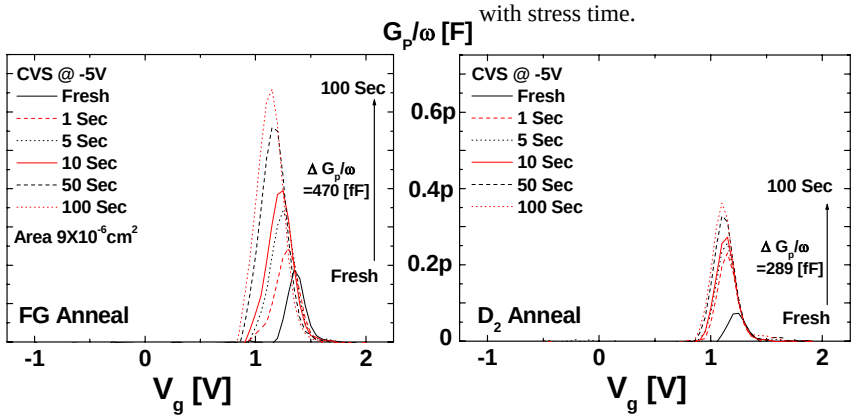

Fig. 5 Conductance loss peak(G_p/ω) Vs. gate voltage(V_g) curve in (a) FG annealed and (b) D_2 annealed samples. D_2 annealed sample shows less interface trap generation than FG annealed sample under same electrical stress.

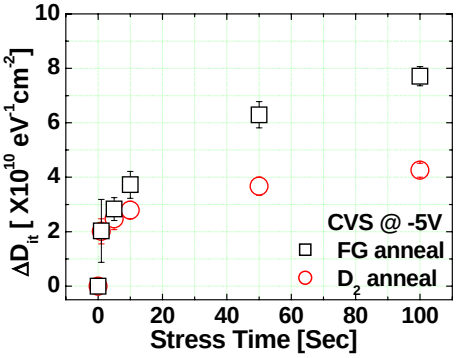

Fig. 6 Interface trap density shift(ΔD_{it}). The reduced interface trap generation under the same electrical stress is shown in D_2 annealed sample.

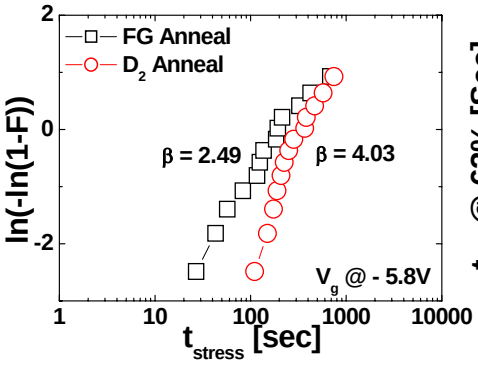

Fig. 7 Weibull distribution of FG and D_2 annealed samples. Deuterium annealed samples exhibited improved Weibull slope β values.

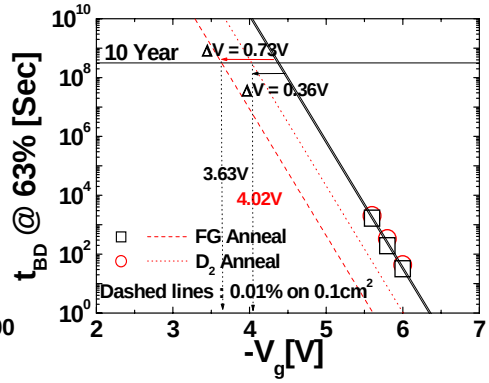

Fig. 8 10 year life time projection of FG and D_2 annealed samples. Solid lines represent 63% failure on 900 μm^2 and dashed lines represent 0.01% failure on $0.1cm^2$.

	V_g	-5.6V	-5.8V	-6.0V
β (Weibull slope)	FG Anneal	2.76	2.49	3.24
	D_2 Anneal	5.60	4.03	5.82
t_{BD} @ 63% [Sec]	FG Anneal	1673	193	32
	D_2 Anneal	1977	329	43

Table 1 Weibull slope(β) and time-to-breakdown (t_{BD} @ 63%) for various stress bias conditions. The weibull slope of deuterium annealed sample is approximately 80% higher than that of control sample.