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0.18 μm Embedded FRAM Fabrication Process and its Consistency with Conventional Logic LSI Process

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1. Introduction

FRAM (Ferroelectric random access memory) is one of the most promising candidates for non-volatile memories of multi-application IC cards and SoC (Systems on a chip) [1,2]. According to ITRS2001 [3], ferroelectric capacitors of 0.18 μm and more advanced technology nodes are required for higher switching performance with smaller capacitor area than those of conventional technology node. In order to realize commercial FRAM, ferroelectric properties related to reliability, i.e. endurance, retention and imprint, are essential. Furthermore, it is also important for process integration to adjust CMOS logic processes to suppress ferroelectric degradation.

In this paper, we describe a ferroelectric capacitor fabrication process for high reliable 0.18 μm FRAM and its compatibility to conventional CMOS logic process.

2. 0.18 μm embedded FRAM technology

Ferroelectric capacitor process

Since we employed almost the same process as a 0.18 μm logic LSI process to fabricate our 0.18 μm FRAM except for ferroelectric capacitor as shown in figure 1, we can use basically the same electric parameters to design our 0.18 μm embedded FRAM. This is an advantage for our FRAM to be embedded on logic LSI without any particular design changes.

Figure 2 and Table 1 show schematic view and specification of 0.18 μm FRAM [4]. Ferroelectric capacitors of IrOx/MOCVD PZT/Ir are made on an Ir barrier layer. High temperature one mask etching technique is also employed to fabricate high aspect capacitors for high density memory. Another advantage of one mask etching is to reduce fabrication costs. It is also possible to fabricate FRAM embedded memory with two additional masks, in contrast to the 6 or more masks that are required for embedded DRAM and embedded FLASH memory. Furthermore, although FLASH memory and EEPROM need high voltage generator which increases chip area, FRAM can be operated without additional high voltage generator. An Ir barrier layer is adopted to suppress W plug oxidation in the case of O_2 atmospheric thermal annealing during ferroelectric capacitor fabrication.

Compatibility with back end process

Figure 3 shows the switching charge at 1.8 V after capacitor fabrication, Metal 1 and Metal 3. A switching charge of 35 μC/cm^2 obtained with 50 μm square capacitor area. Switching performance of the cell arrays consisting of 1.5 μm^2 capacitors does not change from Metal 1 to Metal 3. We do not find any degradation of ferroelectric properties during the conventional back end process. Figure 4 shows cell signal distribution of 512K bit FRAM using 0.35 μm design rule. Widely separated “1” and “0” signal separation of 700 mV at 2.1V guarantees high reliability of our FRAM with BGS (bitline ground sensing) architecture [5].

Compatibility with front end process

During ferroelectric capacitor fabrication processes, CMOS transistors are exposed to a maximum temperature of 600°C. Figure 5 shows W plug contact resistance with and without the Ir barrier layer. The W plug resistance increases during the ferroelectric capacitor fabrication process without the Ir barrier layer. On the contrary, the W plug resistance is constant when using the Ir barrier layer. The W plug oxidization cannot be observed with the Ir barrier. Figure 6 shows $CoSi_2$ – Metal 1 contact resistance. The contact resistance between $CoSi_2$ and Metal 1 does not change from the contact resistance of conventional CMOS thermal budget. It is shown that our ferroelectric capacitor fabrication process need not modify the front end process of logic LSI.

3. Summary

We developed key technologies of ferroelectric capacitors fabrication process, such as MOCVD PZT, high temperature one mask etching, and an Ir barrier layer for 0.18 μm FRAM embedded LSI. Since our developed technologies has been shown to be consistent with conventional CMOS front end process and back end process, our embedded FRAM can be realized using conventional CMOS logic process in addition of only ferroelectric capacitor process.

References

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[3] S. Kawamura et al., International Technology Roadmap for Semiconductor 2001, Front end Process.
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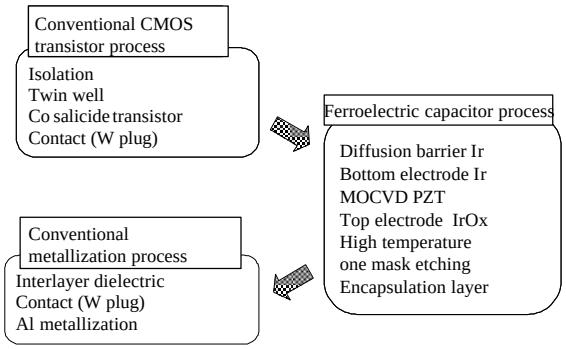

Fig.1. Process flow of 0.18 *m*m embedded FRAM. Ferroelectric capacitor process is inserted between conventional CMOS transistor process and metallization process.

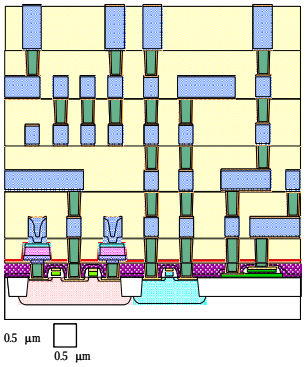

Fig. 2. Cross sectional structure of 0.18 *m*m FRAM.

Table I. Device feature of 0.18 *m*m FRAM

Design rule	0.18 *m*m
Operation voltage	1.8 V
Access speed	30 nsec
Endurance	10^{13} cycles
Cell configuration	1T/1C
Cell area	1.3 *m*m^2
Capacitor area	0.5 *m*m^2
Diffusion barrier	Ir
Bottom electrode	Ir
Ferroelectrics	MOCVD PZT
Top electrode	IrOx
Metallization	5 layer Al/W plug

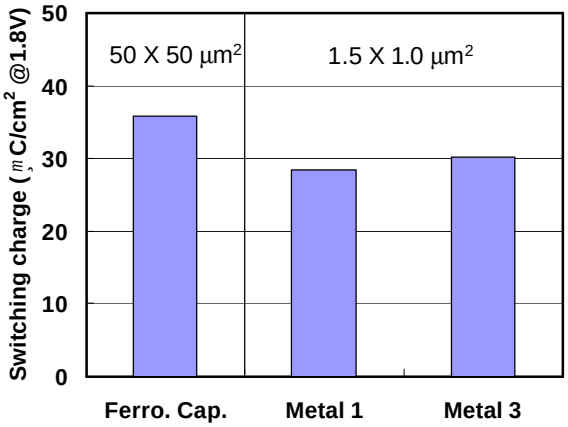

Fig.3. Switching charge comparison after capacitor fabrication, Metal 1 and Metal 3 etching. Capacitor area is 50 X 50 *m*m^2 at capacitor fabrication and 1.5 X 1.0 *m*m^2 at Metal 1 and Metal 3. No process degradation is observed after Metal 1.

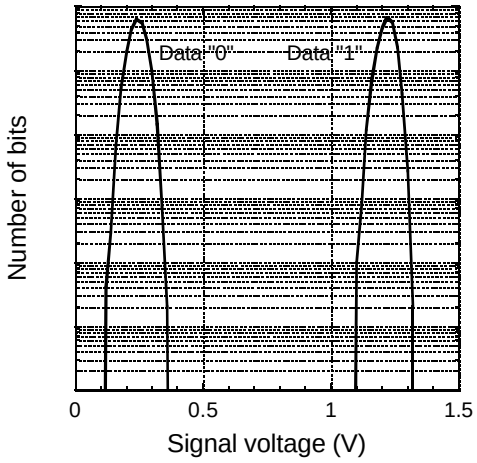

Fig.4. Signal voltage distribution of 512Kb FRAM. Capacitor area is 2*m*m^2. Applied voltage is 2.1V. It is obtained 700 mV data separation, which guarantees reliable FRAM operation.

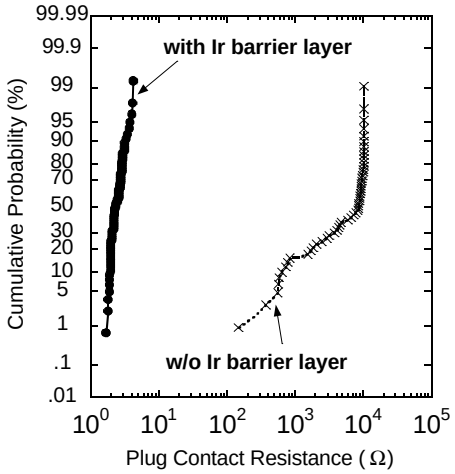

Fig.5. Distribution of plug contact resistance on the capacitors with Ir barrier and without Ir barrier. Stable plug contact resistance are obtained with Ir barrier layer.

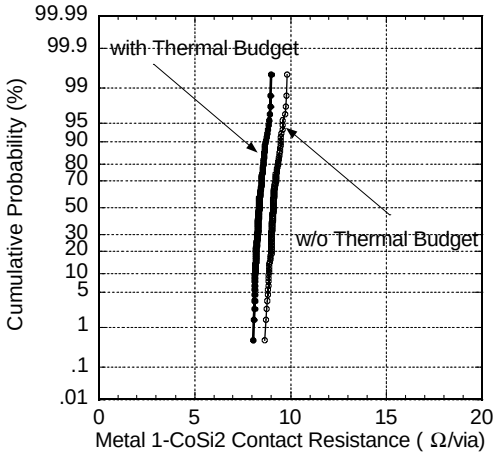

Fig.6. Distribution of Metal 1 – $CoSi_2$ contact resistance. Metal contact is stable after ferroelectric capacitor fabrication process.