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W-Polymetal Gate with Low W/Poly-Si Interface Resistance for High-Speed/High-Density Embedded Memory

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1. Introduction

Embedded or white DRAMs with W-polymetal gates have been reported [1-11]. W-polymetal structure realizes low resistance gate electrode without increase in the aspect ratio compared with WSi or TiSi, so that the number of columns per word line can be reduced, which lead to shrunk chip size. Since W-polymetal also matches with SAC (self-aligned contact) process, it is suitable for high-density memories.

W-polymetal gate needs a barrier layer between W and poly-Si in order to suppress silicidation of W. WN and TiN are reported as barrier metal. Gate re-oxidation has the advantages of enhancement of gate-oxide integrity and suppression of GIDL (gate induced drain current). In the case of WN, gate re-oxidation can be adopted by selected oxidation in H_2O/H_2 mixed ambient. In this point of view, WN barrier is desirable.

In this paper, the contact resistance between W and poly-Si is discussed. Fig. 1 shows the dependence of relative delay time of CMOS inverter with the contact resistance between gate-metal and poly-Si. Constant resistance is assumed to be ohmic in Fig. 1. The contact resistance greatly affects for logic circuits with high-speed operation. We find the contact resistance becomes non-ohmic and considerably high for the W/WN/poly-Si structure, though the low contact resistance estimated from sheet resistance of polymetal gate has been reported [1]. New W-polymetal gate structure with low W/poly-Si interface resistance is proposed.

2. Experimental

Fig. 2 shows the process flow. After gate oxidation and poly-Si deposition, gate doping is performed for NMOS and PMOS. Then PVD-WSi of 10-nm-thick is deposited and RTA is performed. Another two samples are fabricated as references: one is the sample without WSi, and the other is the sample with WSi insertion and no RTA treatment. In-situ WN and W are deposited in Ar/N and Ar ambient, respectively. Thickness of WN and W are 5 nm and 40 nm, respectively. SiN is deposited as a cap layer and a hard mask for gate etching. After gate definition, furnace gate re-oxidation is performed in H_2O/H_2 ambient to oxidize poly-Si selectively. Then S/D and SiN-sidewall are formed by conventional process. For measurement of the contact resistance between W and poly-Si, a part of W is etched using additional mask to make Kelvin patterns.

3. Results and Discussion

Gate Resistance

Fig. 3 shows a cross-sectional SEM image of W/WN/WSi-polymetal gate with selective oxidation. Dependences of sheet resistance of gate electrode on line width are shown in Fig. 4. While the resistance of WSi-polycide gate increases rapidly at the region of $Lg < 0.2$ μm, W-polymetal gate maintains low resistance until the region of $Lg < 0.1$ μm. The advantage of polymetal gate is clearly shown. Fig. 4 also shows that good selectivity is kept on gate re-oxidation.

Contact Resistance

Contact resistance between W and poly-Si is shown in Fig. 5 as a function of current density. In the case of conventional W/WN/poly-Si, contact resistance becomes considerably high especially at small current density. In our CMOS-inverter delay estimation using non-linear contact resistance model, this non-ohmic resistance increases delay time by 20 %. On the other hand, for our new structure of W/WN/WSi/poly-Si, the contact resistance remains low irrespective of current density. Fig. 6 shows the distribution of the contact resistance. Closed symbols and open ones are resistance at the current density of 0.1 $\mu A/\mu m^2$ and 1 $\mu A/\mu m^2$, respectively. Split of closed symbol and open symbol means non-ohmic resistance. W/WN/poly-Si gate shows non-ohmic characteristics with less variation. For polymetal gate with WSi insertion and no RTA treatment, the contact resistance is still non-ohmic and large variation. RTA treatment immediately after WSi deposition gives ohmic and stably low contact resistance. Cross-sectional TEM images are shown in Fig. 7. Unexpectedly, nothing like dielectrics is observed at the boundary of W and poly-Si for W/WN/poly-Si. On the other hand, for W/WN/WSi/poly-Si, agglomerated WSi in the shape of islands is observed, which is considered to keep electric contact between W and poly-Si intermittently.

Transistor characteristics

Fig. 8 shows inter-diffusion of dual gate. Large shift in threshold voltage is observed for W/WN/WSi without RTA. In this case, continuous WSi structure is still considered to be remaining. RTA modifies the WSi structure and almost no shift occurs for W/WN/WSi/poly-Si as well as W/WN. *Vg-Id* characteristics of MOSFET are shown in Fig.9. It can be seen that insertion of thin-WSi does not cause any adverse effect.

4. Conclusions

W-polymetal gate with the structure of W/WN/WSi/poly-Si is newly proposed. Ohmic and sufficiently low contact resistance between W and poly-Si is obtained by deposition of thin-WSi on poly-Si and following RTA. This process is promising for high-speed and high-density embedded memory.

References

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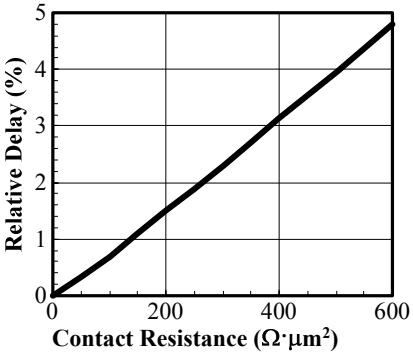


Fig. 1. Dependence of relative CMOS-inverter delay on contact resistance between gate metal and poly-Si.

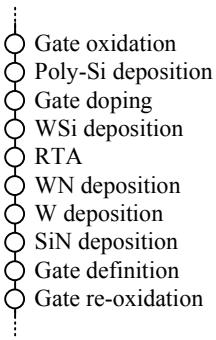


Fig. 2. Process flow.

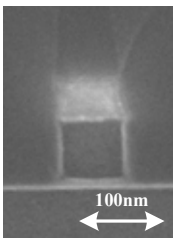


Fig. 3. Cross-sectional SEM image of W-polymetal gate.

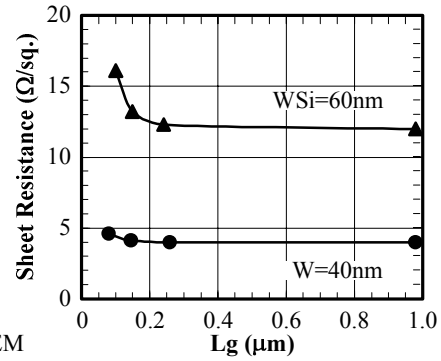


Fig. 4. Dependence of sheet resistance on line width for W-polymetal and WSi-polycide gate after gate re-oxidation.

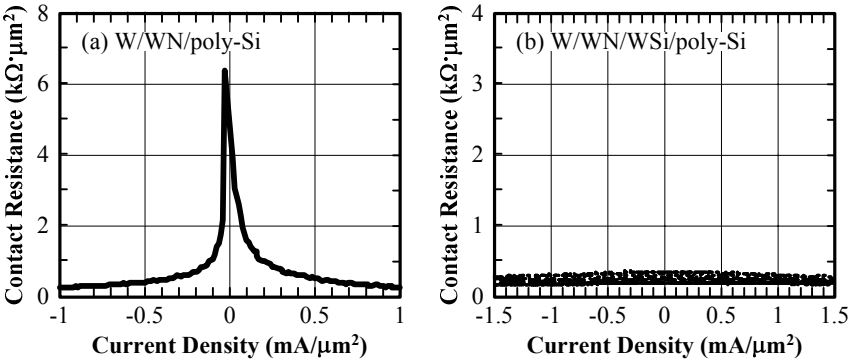


Fig. 5. Contact resistance between W and poly-Si for W-polymetal gate with and without thin-WSi on poly-Si as function of current density.

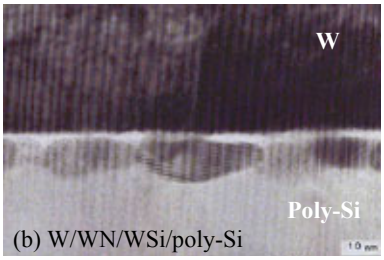
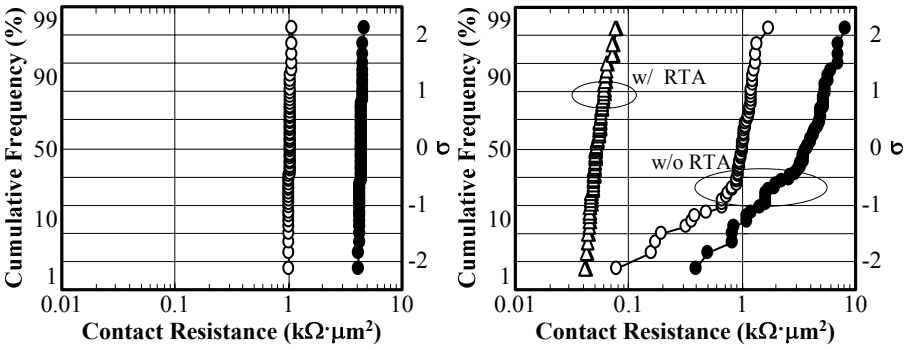


Fig. 7. Cross-sectional TEM image of interface between W and poly-Si for polymetal gate with and without thin-WSi on poly-Si.



(a) W/WN/poly-Si (b) W/WN/WSi/poly-Si

Fig. 6. Distribution of contact resistance between W and poly-Si. Closed symbol shows current density of 0.1μA/μm² and open symbol shows 1μA/μm².

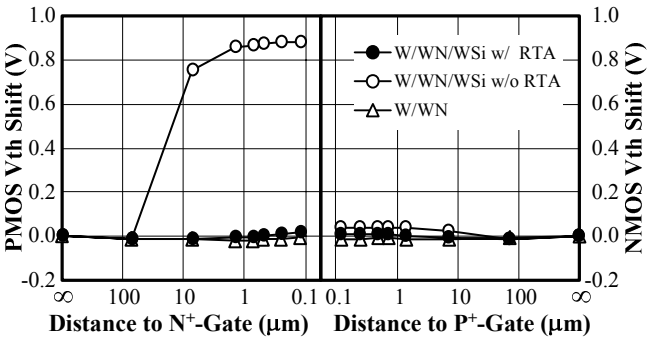


Fig. 8. Inter-diffusion of W-polymetal gate.

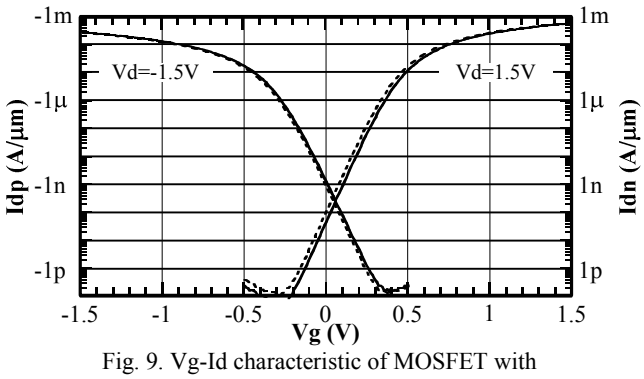


Fig. 9. Vg-Id characteristic of MOSFET with W/WN/WSi-polymetal gate.