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Silicon Selective Epitaxial Growth for Self-Aligned Cell Contact Featuring High Performance Sub-100nm DRAM Cell Transistors

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Introduction

High performance requirement for the DRAM cell transistors is important in recent technology node of production since the market continuously needs the faster devices. A recent trend of failure modes also shows that the low saturation current (I_{DSAT}) of the cell transistor is a yield determining factor in DRAM, see Fig. 1[1]. Therefore, developing a new process which improves the I_{DSAT} is a critical issue for the DRAM fabrication.

Parasitic resistances such as lightly doped drain (LDD) resistance and pad to N- contact resistance (pad/N- R_{CNT}) become significant as the device is scaled down, in Fig. 2. Several literatures were devoted to estimate and reduce these parasitic resistances[2,3,4], and applying an elevated source/drain (E-S/D) using silicon selective epitaxial growth (Si-SEG) is suggested as a method to decrease the pad/N- R_{CNT}, which makes possible to heavy implant on Si-SEG layer to reduce the pad/N- R_{CNT}[4]. However, the E-S/D growth for the DRAM cells after gate patterning has some critical issues such as bridging of adjacent Si-SEG layers and microloading effect.

In this paper, Si-SEG applied after self-aligned contact (SAC) opening in the scaled DRAM process, referred as SAC-SEG process, is introduced to overcome the shortcomings of E-S/D and to improve the performance of DRAM cell transistor, and the properties of the cell transistor with the SAC-SEG process were investigated.

Experiment

DRAM cell with 0.14μm design-rule was fabricated following the SAC-SEG process as shown in Table I and Fig. 3. The gate stack was consisted with poly-Si/WSix and 68Å thick gate oxide. After the SAC etching, the Si-SEG was proceeded using UHV-CVD system at low process temperature (~700°C) with thickness up to about 500Å. The same processes with the conventional, except the heavy doping on the Si-SEG to reduce the R_{CNT} (~10^{15}/cm^2), were followed after the Si-SEG.

Results and discussion

Fig. 4 shows the cross-sectional SEM images of the DRAM cell just after the SAC-SEG process. It can be clearly seen that the bridging problem of the E-S/D between storage nodes was prohibited by the ILD walls as shown in Fig 4(c). The electrical characteristics for the SAC-SEG process compared to the conventional process (without the SEG) were shown in Fig. 5 to Fig. 7.

A salient feature for the cell transistors with the SAC-SEG is a 25% increase of the drain current, measured at V_D=V_G=2V, with respect to the conventional one as shown in the I_D-V_D curves of Fig 5(a); but the threshold voltage and its distributions estimated from the I_D-V_G measurements for the two samples were quite the same as shown in Fig. 5(b) and the insert of Fig. 5(b). This means that the difference of the I_{DSAT} can be attributed to the parasitic effect such as the R_{CNT}. Fig. 6 shows more clearly that the I_{DSAT} increase was originated from the improvement of the pad/N- R_{CNT}. The distribution of the pad/N- R_{CNT} in Fig. 6(b), which were measured under the forward biased drain to p-well diode of the cell transistors, shows significant difference between the two samples and it traces the I_{DSAT} distributions of Fig. 5(a) very well; this is a strong evidence for the I_{DSAT} increase due to the pad/N- R_{CNT} reduction.

Another important feature for the SAC-SEG process is the no increase in the short channel effect (SCE) which is represented by the drain induced barrier lowering (DIBL) as shown in Fig. 5(b), in spite of the heavy doping on the Si-SEG to reduce the contact resistance. Since the pad contact was formed at about 500Å above the level of the transistor channel, diffusion of the dopant toward the channel was retarded by the elevated SEG layer and consequently leads the smaller DIBL. This is a good signature in applying the SAC-SEG process for the further scaled DRAM cells.

The breakdown voltages, defined by the drain voltage for 10nA leakage current under the gate turned-off, for the cell transistors with the SAC-SEG process decrease slightly (~3%) compared to the conventional process, in Fig. 7, showing the slight increase of leakage current at the voltage region higher than operation; it can be attributed to the band-to-band tunneling at the gate edge of the drain junction due to the heavy doping. However, the difference in the source to drain (S/D) leakage current estimated in the subthreshold region from the Fig. 5(b) for the two samples is negligible.

Conclusion

The SAC-SEG process was applied in DRAM to increase the performance of the cell transistors and the characteristics were investigated in detail. Compared to the conventional process, the SAC-SEG leads 25% increase of drain current, which resulted from reduction of pad/N- R_{CNT} without affecting threshold voltage, DIBL, and S/D leakage current. The SAC-SEG process can be suggested for sub-100nm high performance DRAM cell contacts.

References

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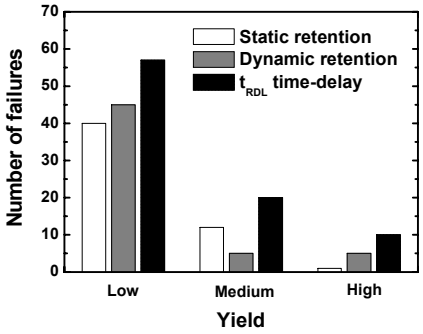


Fig. 1. Trends of the number of failures for three major failure modes of the recent DRAM product. The t_{RDL} which directly depends on the I_{DSAT} is a dominant factor.

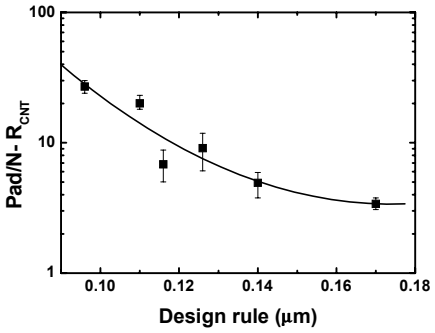


Fig. 2. Contact resistance for the DRAM cell contacts as a function of the design-rule.

Table 1. The SAC-SEG process sequence.

* Shallow trench isolation
* Well and channel formation
* Gate(poly-Si/WSi_x) patterning
* ILD deposition and CMP
**** Self aligned contact etch***
**** Elevated S/D SEG formation***
- UHV-CVD SEG (700℃)
**** Cell SEG implantation***
* Cell pad(poly-Si) formation
* W Bit line formation

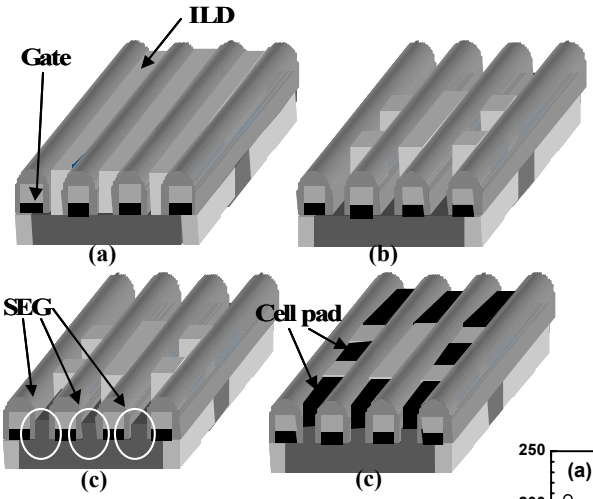


Fig. 3. Schematic diagrams for the SAC-SEG process flow. (a) the first ILD layer was deposited, (b) cell contacts were opened by SAC etch, (c) after the SEG, (d) cell pad poly was deposited. Bridges between the storage nodes can be prohibited by the ILD layers in the SAC-SEG process.

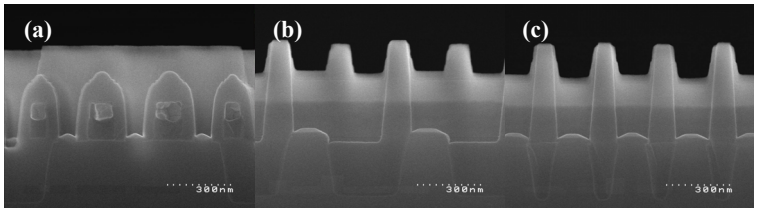
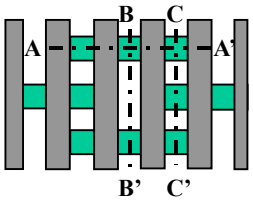


Fig. 4. Cross-sectional SEM images for the DRAM cells. (a) cross-section cut along the bit-line direction (A-A'), (b) along the word-line direction through direct contacts (DC)(B-B'), (c) word-line direction through storage nodes (C-C'). The right hand side drawing shows active and word-lines.



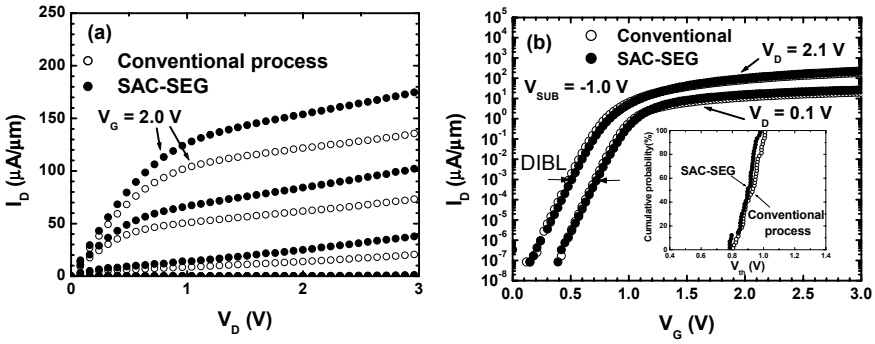


Fig. 5. Saturation current and sub-threshold characteristics for the cell transistors fabricated using the conventional process (without SEG) and the SAC-SEG process. (a) saturation current characteristics. (b) sub-threshold characteristics. Insertion: distribution of the threshold voltages for the two samples.

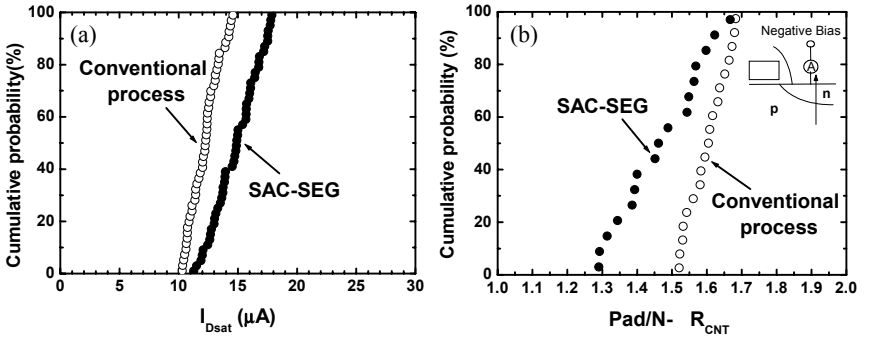


Fig. 6. Saturation current and contact resistance distributions. (a) saturation current distribution, (b) contact resistance distribution. The figures clearly show that the I_{DSAT} increase for the SAC-SEG was originated from the R_{CNT} reduction.

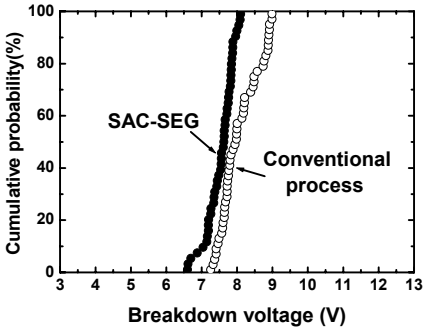


Fig. 7. Breakdown voltage distribution, drain voltages for 10nA source-to-drain leakage current at the off-state, for the SAC-SEG and conventional process.