

## Optimum $\text{TiSi}_2$ Ohmic Contact Process for Sub-100nm Devices

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### 1. Introduction

$\text{TiSi}_2$  has become the most widely used ohmic layer in advanced logic and DRAM devices due to its low resistivity, excellent thermal stability and ability to be formed by in-situ PE-CVD Ti deposition process<sup>[1,2]</sup>. However, recently we observed that junction leakage current was rapidly increased in small contacts due to a direct contact (DC) defect which was generated at DC sites after W bit-line formation.

In this paper, we studied the cause of increase in the junction leakage current and DC defect at small contacts. The mechanism responsible for generation of the DC defect was suggested by analysis of defect structure, and method for prevention of such defect was recommended in below 100nm devices.

### 2. Experimental

In this study, we focused on n+/p shallow junctions because they cause more severe leakage current. In order to investigate the n+/p junction leakage current in various contact sizes, devices with below 100nm design rules was utilized with a special emphasis on the DC. The trend of the DC defect was investigated by varying thermal budget from 700°C to 900°C before LP-SiN process for bit-line formation. In the DC process, Ti/TiN barriers were deposited by in-situ PE-CVD Ti and CVD-TiN, and W plug was deposited on TiN for acceptable small contact formation. The bit-line spacer was constructed through LP-SiN process at 680°C for 5 hours, which was the first thermal budget after the DC and bit-line formation. The capacitor process was carried out and finally metal contact and metal layer were fabricated.

The junction leakage current was measured at 75\*75  $\mu\text{m}$  area patterns with 10k contacts. TEM and EDX were used to evaluate structural and qualitative analysis of the DC defect, respectively. XRD was also carried out to analyze Ti-silicide transformation after thermal budget.

### 3. Results and Discussion

Fig.1 shows the n+/p junction leakage current at 0.11 $\mu\text{m}$  and 0.16 $\mu\text{m}$  contact size. As the contact sizes decreased, portion of extremely high leakage current increased. We investigated the mechanism of the high leakage current by evaluating I-V characteristics of the n+/p junction under reverse bias as shown in Fig. 2. In case of defect free contacts, Fig. 2-a, as measurement temperature was increased from 25°C to 100°C, n+/p junction leakage current was increased with increasing temperature with similar slope, respectively. Fig. 2-b shows the I-V curve of n+/p junction with thicker  $\text{TiSi}_2$ . Although the values of the leakage currents are substantially increased, the general shape of the leakage current curve was similar to that of the defect free contact, suggesting the same current conduction mechanism. But, in case of Fig. 2-c, the leakage current became independent of the measurement temperature and the same value of the current was

observed above 1V, which can be attributed to tunneling mechanism.

To reveal the cause of the leakage failure in Fig. 2-c, TEM analysis was conducted. As shown in Fig. 3-a, an abnormally grown dark region was observed at the bottom of contact which was distinguished from  $\text{TiSi}_2$ . In Fig. 3-b, the diffraction pattern of dark region resulted in the same zone-axis of Si [100] and [200]. EDX analysis showed that Si:Ti ratio was above 20:1. Therefore, we could conclude that the defect is a Si defect such as interstitial loop or dislocation in which contains diffused Ti. In addition, we assumed that the dark contrast is a result of Ti diffusion into the defect area<sup>[2]</sup>.

Defect generation step was illustrated in Fig. 4. After the first thermal budget step at 680°C for 5 hours during LP-SiN formation, the leakage current was increased. Although a higher thermal budget of about 750°C 30min was applied after LP-SiN deposition, the level of leakage current was unchanged. In previous reports, increased junction leakage current by Co-silicide formation was improved after applying higher thermal budget, because abnormal  $\text{CoSi}_x$  spikes, which were generated in a relatively low thermal treatment<sup>[3]</sup>, were removed in that case. However, high leakage current due to DC defect in this study was not improved in spite of applying thermal treatments after LP-SiN.

XRD analysis as shown in Fig. 5-a for phase transformation of Ti-silicide with thermal budget was investigated at the same thickness of Ti as in contact application. As-deposited and 700°C RTN treated Ti-silicides were mainly observed as  $\text{TiSi}(211)$  and  $\text{C49-TiSi}_2(131)$ , but  $\text{C54-TiSi}_2(311)$  was mainly detected after 900°C RTN. It is more difficult for thin  $\text{C49-TiSi}_2$  to transform to  $\text{C54-TiSi}_2$  at the same thermal budget as shown in Fig. 5-b.

Therefore, we have concluded that Ti diffusion into the Si defect site occurred for insufficient thermal energy in small contact. So, sufficient thermal treatment, just after barrier metal deposition, could prevent junction leakage current by transformation of  $\text{C54-TiSi}_2$  from  $\text{C49-TiSi}_2$  phases. Finally, sufficient thermal treatment was applied before LP-SiN and we have perfectly improved the junction leakage current at 100nm devices as shown in Fig. 6.

### 4. Conclusion

We detected the DC defect that was responsible for the high leakage current that became severe as decrease contact size. The defect was generated by unstable phase transformation of  $\text{C49-TiSi}_2$  to  $\text{C54-TiSi}_2$  during the first thermal process and Ti diffusion at Si defect sites. A successful integration of the DC is achieved by using higher thermal treatment before LP-SiN process because sufficient thermal treatment could transform  $\text{C49-TiSi}_2$  to  $\text{C54-TiSi}_2$  phase at DC contact bottom.

## 5. References

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 [2] D. S. Wen et al, *Appl. Phys. Lett* 51(15), p1182, 1987  
 [3] K. Goto et al, *Transc. on Elect. Devices*, v46, n1, p117, 1999.

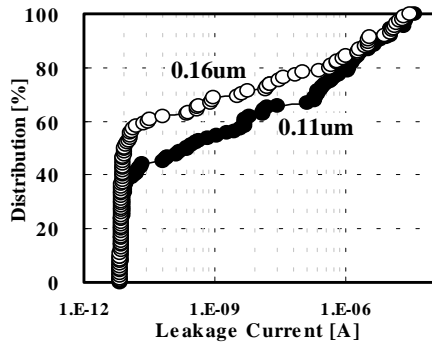


Fig. 1. n+/p junction leakage current at 0.11um and 0.16um contact sizes.

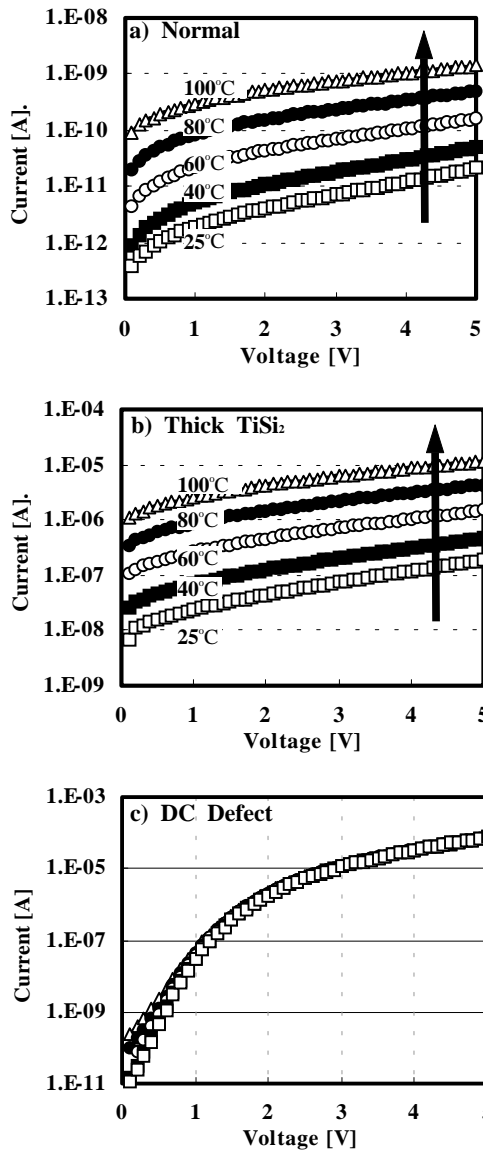


Fig. 2. Characteristics of n+/p junction leakage current with various measurement temperatures.

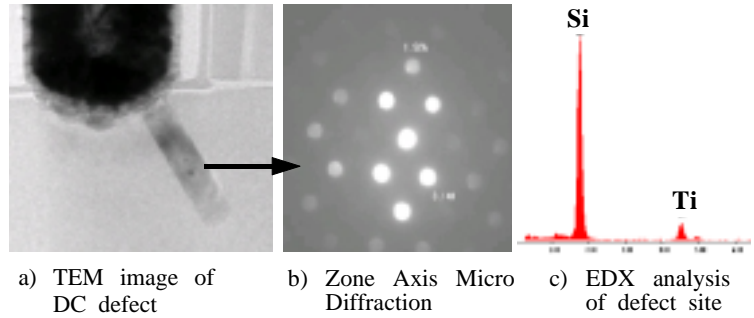


Fig. 3. TEM & EDX analysis at defect site.

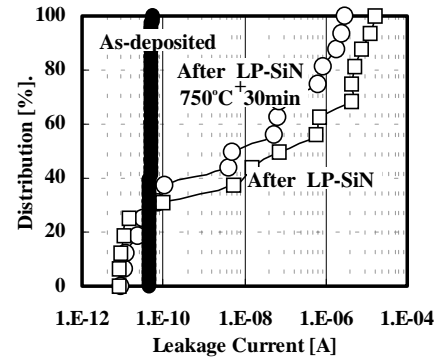


Fig. 4. n+/p junction leakages current after various thermal budget.

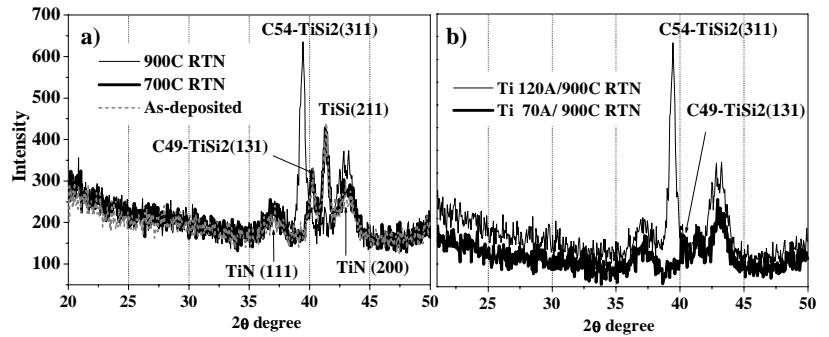


Fig. 5. XRD analysis of Ti-silicide for a) various thermal budget and b) different Ti thickness with the same thermal budget.

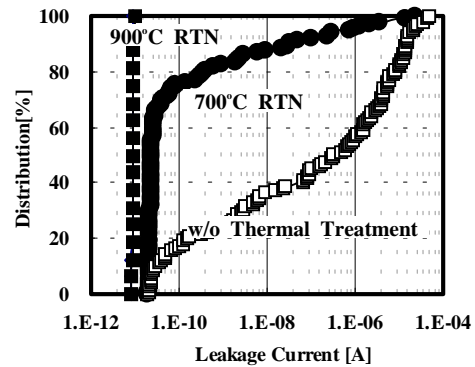


Fig. 6. n+/p junction leakage current for post thermal treatment before LP-SiN process