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Pt/BST/Pt Capacitor Technology for 0.15㎜ Embedded DRAM

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Abstract

Pt / BST / Pt capacitor technology has been developed for 0.15 μm embedded DRAM. The CVD/sputter-BST process is established with high reliability. Moreover, both of thermal stability (budget) and reductive stability of the BST capacitors are improved by introducing modulated oxygen-doping into the Pt top electrode. This BST capacitor has been integrated into the 0.15μm embedded DRAM having a CUB (Capacitor Under Bit-line) structure and 4-levels metallization.

1. Introduction

Embedded DRAM technology is important to realize a system-on-a-chip. BST capacitors are suitable for embedded DRAM because of the low temperature process. This feature should be more desirable as embedded DRAM performance become higher. However, the BST capacitor has some issues for the device integration. One of the most serious issues is the degradation in the back-end process. This paper reports a solution which is concerned with a new top electrode structure.

2. Experimental

Figure 1 shows the BST capacitor TEG (Test Element Group) structure. The Pt side-walled bottom electrodes characterize the BST capacitor TEG. The cell size is 0.46 μm x 0.96 μm and, the typical bottom electrode size is 0.30 μm x 0.70 μm. Typically the 50 nm BST was deposited on the 200 nm-high Pt side-walled bottom electrode with 128 kbits-scale integration.

Figure 2 shows the process flow of the BST capacitor TEG. The film of BST was consisted of a bulk CVD-BST layer and a sputter-BST liner as a blanket nucleating layer[1]. The Pt electrodes of the capacitor were formed by sputtering in argon and oxygen mixture gas so as to decrease the leakage current. Especially oxygen doping into top Pt electrodes improves reductive stability effectively[2].

3. Results and Discussions

A. Characterization of CVD/sputter-BST capacitor

Figure 3 shows the cross-sectional SEM photograph of the BST capacitors. A film of BST on the sidewall surface is half as thick as one on the top surface of the bottom electrode.

One of the important process in this CVD/sputter-BST is the sputter-BST liner formation. Figure 4 shows the leakage current of the BST capacitor TEG connecting the bottom electrodes to the ground, and figure 5 shows the capacitance of them. They are depending on the annealing temperature of the sputter-BST liner. The leakage current increases fatally with 675ºC N_2 annealing. On the contrary, the capacitance decreases with 575ºC N_2 annealing. Around 625ºC N_2 annealing may be suitable. Figure 6 shows TDDB characteristics of the BST capacitors. The extrapolated 63.2% lifetimes are more than 10 years.

B. Improvement of thermal stability

Another issue is poor thermal stability of the BST capacitor. Recent metallization process including CVD TiN and/or HDP CVD SiO_2 needs about 500ºC process temperature. To overcome this difficult problem, we designed modulated oxygen-doped Pt electrodes, which were formed by a sequence of sputtering in low oxygen ambient and sputtering in high oxygen ambient . Figure 7 shows the leakage current characteristics of the BST capacitors with the top above-mentioned Pt electrodes. The BST capacitors with the modulated top Pt electrodes show the lower leakage current properties than the conventional monotonous top Pt electrodes.

Next, the degradation caused by reduction of the BST capacitor was evaluated. Figure 8 shows the leakage current characteristics of the 40 nm CVD/sputter-BST capacitor after both of N_2 annealing and H_2 annealing. The degradations are observed especially positively biased. In this case, the leakage current is affected by the electron injection from the top electrode. Because the interfacial BST may be reduced by hydrogen, the leakage current increases. However, the leakage currents are less than 1 fA/cell under both the +0.8V bias and the -0.8V bias. Figure 9 shows the cumulative probability plot of the capacitance of the BST capacitor as shown in Figure 8. The capacitance of 15 fF/cell are obtained in the almost chips.

It is noteworthy that only changing the oxygen concentration in the top Pt electrode brings out the drastic improvement.

C. Integration of embedded DRAM

The newly developed BST capacitor has been integrated in the embedded DRAM. Figure 10 shows the process flow. Figure 11 shows the cross-sectional SEM photograph of the embedded DRAM with BST capacitor. TiN bottom electrode contact plug, a CUB structure and a 4-levels metallization characterizes this embedded DRAM. The BST capacitors are compatible for the CUB structure because of their low height. However, the CUB structure has the bit line contact-holes through the top electrode and the BST. The poor etchability has been broken through with new high-temperature Pt etching technology using hard mask.

4. Conclusion

The CVD/sputter-BST capacitor with more than 10 years lifetime has been developed. The BST capacitor maintains the low leakage current and the enough capacitance after back-end process including both of N_2 annealing and H_2 annealing. The embedded DRAM with the BST capacitor has been successfully integrated for the first time.

5. References

[1] H. Itoh et al., Symp.on VLSI Tech., p. 106 (2000).
[2] Y.Tsunemine et al., IEDM Tech. Dig., p. 811 (1998).

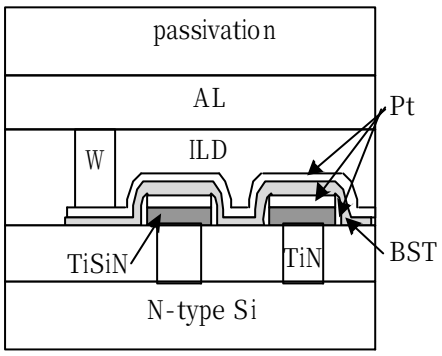

Fig. 1. Structure of the BST capacitor TEG (Test Element Group) for evaluating the electrical properties.

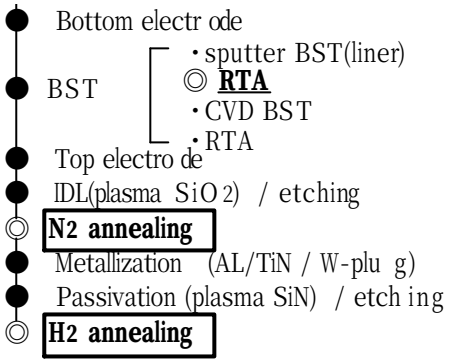

Fig. 2. Process flow of the BST capacitor TEG.

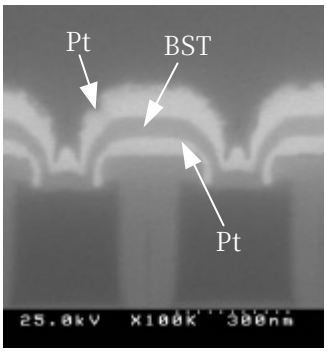

Fig. 3. Cross-sectional SEM photograph of the BST capacitor integrated on the Pt side-walled bottom electrode.

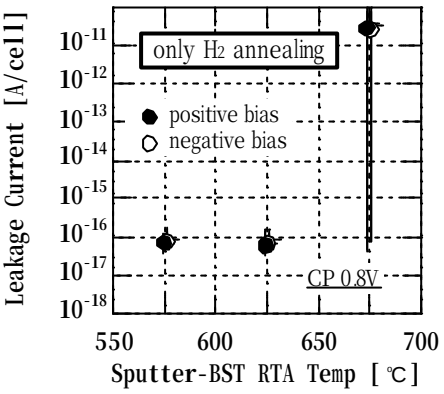

Fig. 4. Leakage current of the integrated BST capacitor after the back-end process with H_2 annealing. (Bars shows the max-min range.)

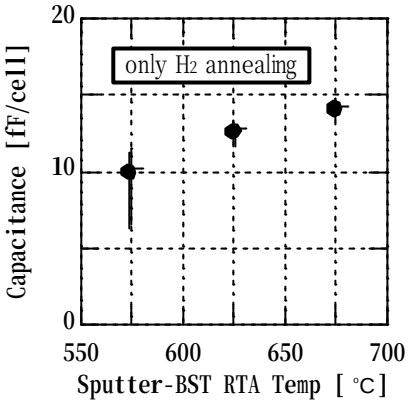

Fig. 5. Capacitance of the integrated BST capacitor after the back-end process with H_2 annealing. (Bars shows the max-min range.)

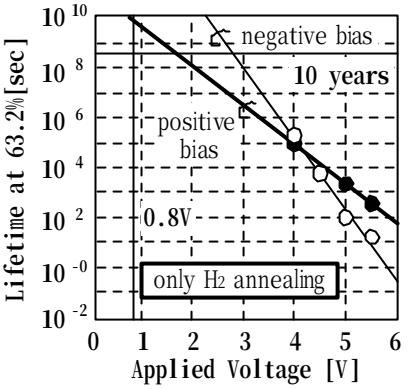

Fig. 6. Breakdown lifetime extrapolation of the integrated BST capacitor with H_2 annealing.

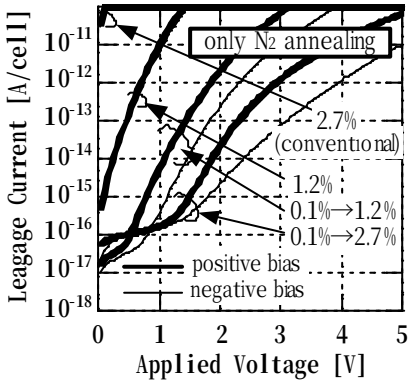

Fig. 7. Improvement in the leakage current of the integrated BST capacitor after the back-end process with N_2 annealing. The percentages are the oxygen contents of sputtering O_2/Ar gas on filming the top Pt electrode.

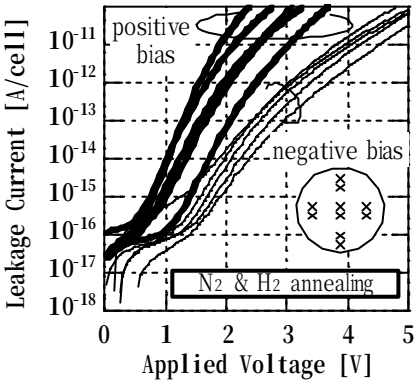

Fig. 8. Leakage current characteristics of the improved BST capacitor fully integrated, the back-end process including both of N_2 annealing and H_2 annealing.

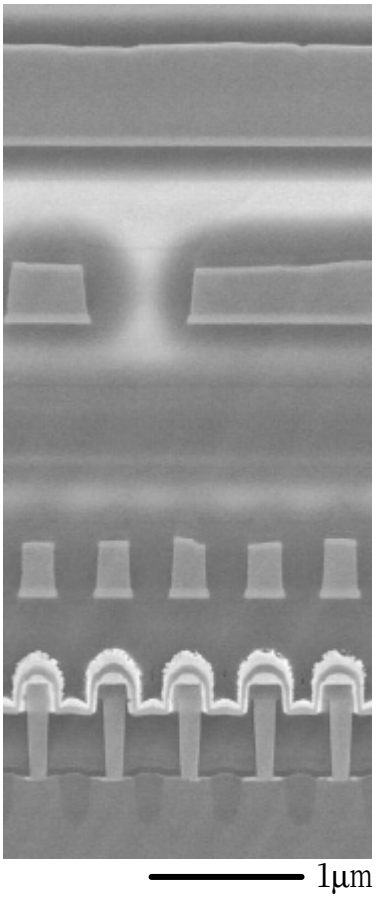

Fig.11. Cross-sectional SEM photograph of the embedded DRAM with BST capacitors.

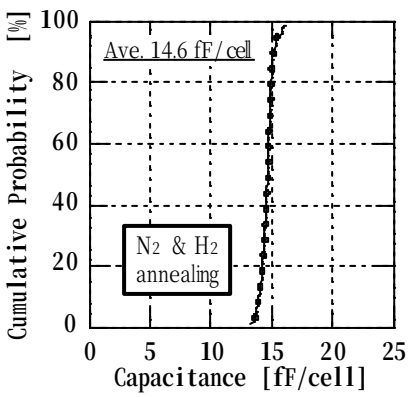

Fig. 9. Capacitance distribution of improved the BST capacitor , the same sample shown in figure 8.

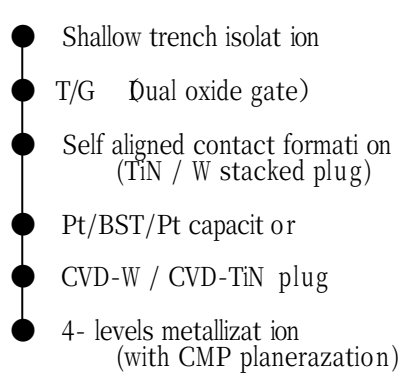

Fig. 10. Process flow of the embedded DRAM.