

Low Resistive Contacts of TiN-Barrier and Ru-Electrode Using PCM Sputtering for MIM-Ta₂O₅ Capacitors in Giga-Bit DRAMs

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1. Introduction

The Ru/Ta₂O₅/Ru (MIM-TaO) capacitor is the most promising in giga-bit DRAMs with design rules of 0.10 μm and below [1], because the Ta₂O₅ film with a low leakage current is easily obtained after an oxidation annealing. However, the contact resistance (R_c) of the Ru storage node (SN) and the barrier metal increases during this annealing, because oxygen ions diffuse through the Ru SN and they oxidize the barrier metal (Fig. 1). Two countermeasures would be considered to reduce the R_c : (i) using oxidation-resistant material as barrier metal, and (ii) preventing oxygen ions from diffusing through the Ru electrode. The sp-TaN barrier has successfully reduced the R_c [2], however there is a problem in scalability to 0.10- μm -design rule because the CVD technique of TaN has not been matured yet.

In this work, we have developed a novel oxidation-resistant Ru-SN electrode fabricated by using the point-cusp magnetron (PCM) sputtering. The PCM sp-Ru film reveals a high bottom coverage and has few grain boundaries, so that oxygen is restrained from diffusing to the barrier metal. Thus, low resistive contacts can be obtained even with a prevalent CVD-TiN barrier. In this paper, we demonstrate the characteristics of the Ru-SN / TiN-barrier contact and its device integration in DRAM cells.

2. Contact Resistance of Ru SN and TiN Barrier

Dependence on Ru Thickness

The R_c was measured by applying 0.5 V between the Ru SN and the TiN barrier (Fig. 2). The low resistive contact of 10 $\text{k}\Omega\cdot\text{bit}$ with a small dispersion was obtained for the PCM sp-Ru, while the R_c was ten times larger for the conventional sp-Ru (Figs. 3 and 4).

Dependence on Ru Grain Boundaries

Figures 5 and 6 show the TEM views of the interfaces of the Ru SN and the TiN barrier. For the conventional sp-Ru, many of grain boundaries have been observed penetrating through the Ru electrode, and titanium oxide (TiO_x) layer has been formed (Fig. 5). It is suggested that oxygen ions diffuse via Ru grain boundaries to form TiO_x. This TiO_x is a cause of high R_c . On the other hand, for the PCM sp-Ru, the Ru film is strongly oriented with few grain boundaries (Fig. 6). Thus, oxygen has been restrained from diffusing to the TiN barrier, so that the R_c has been kept low without TiO_x formation. Accordingly, the R_c is strongly related with the Ru grain boundaries (Fig. 7).

Dependence on Ta₂O₅ Oxidation Temperature

The oxidation process at high temperatures is required to

lower the leakage current of the capacitors below $10^{-8}\text{A}/\text{cm}^2$, while the R_c increases along with the oxidation temperature (Fig. 8). To keep a DRAM operation speed sufficiently high, the R_c should be lowered below 20 $\text{k}\Omega\cdot\text{bit}$. For the conventional sp-Ru, the oxidation temperature is restricted to 360°C, so that the leakage current is over $10^{-6}\text{A}/\text{cm}^2$. By using the PCM sputtering, we have obtained the Ru electrode, which satisfies both the low R_c and the low leakage current at once (at 410°C in Fig. 8).

3. Device Integration & Electrical Properties

Process Flow

We integrated the MIM-TaO capacitors according to the process flow in Fig. 9. The contact holes with a diameter of 0.10 μm were opened by an RIE process, and they were filled with poly-Si. The poly-Si plugs and 100-nm-deep recesses were fabricated by a dry etching. Then, the recesses were filled with CVD-TiN, and the excess TiN film was removed by CMP. An interlayer dielectric (ILD) film, PETEOS-SiO₂, was deposited and the SN holes were opened through the ILD. The Ru films were deposited by the PCM sputtering and consequently by CVD, and they were etched back to form the concave-type SN. Next, the CVD-Ta₂O₅ film was deposited and annealed in O₃ ambient at 410°C for 10 min. Finally, the CVD-Ru top electrode was fabricated.

Electrical Properties

Figure 10 shows the cross-sectional view of the MIM-TaO capacitor. The concave-type Ru electrode was 1.0- μm high with a 0.10- μm design. The capacitance was 13 fF/bit for a 1.0- μm -high capacitor, so that an easily manufacturable 2.0- μm -high capacitor will bring about 27 fF/bit. The leakage current was below $10^{-16}\text{A}/\text{bit}$ in the range of -1 to +1 V at the DRAM operation temperature of 90°C (Fig. 11) with an R_c of 10 $\text{k}\Omega\cdot\text{bit}$. These values are sufficient for the giga-bit scale DRAM applications to ensure their high-speed operations.

4. Conclusions

We have developed a novel oxidation-resistant Ru-SN electrode using the PCM sputtering for MIM-TaO capacitors. This Ru electrode restrains oxygen from diffusing to the TiN barrier, because it has few grain boundaries. Thus, we have obtained the contact resistance of 10 $\text{k}\Omega\cdot\text{bit}$, and the leakage current of $10^{-16}\text{A}/\text{bit}$ (-1 to 1 V) at once.

References

- [1] Y. Ohji *et al.*, *Oyo Butsuri*, 66, (1997) 1210.
- [2] Y. Nakamura *et al.*, *VLSI Symp.*, 2001, p. 39.

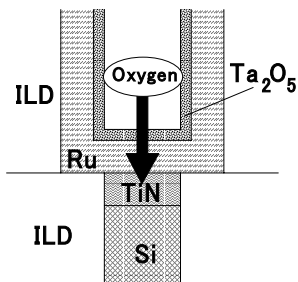


Fig. 1 Schematic view of MIM-TaO capacitor. Oxygen diffuses through Ru and oxidizes barrier.

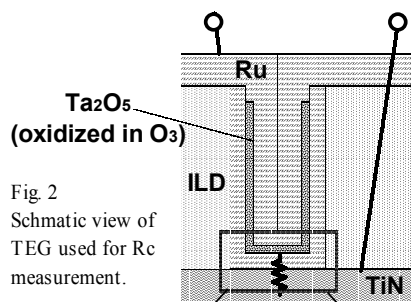


Fig. 2 Schematic view of TEG used for R_c measurement.

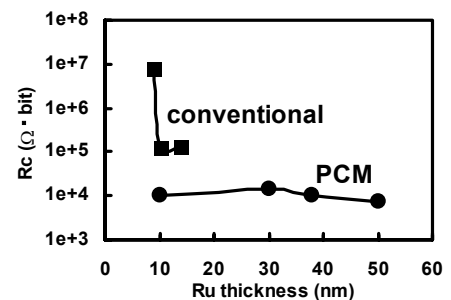


Fig. 3 Contact resistance of Ru / TiN as function of Ru thickness. Oxidation was carried out at 410°C in O_3 ambient.

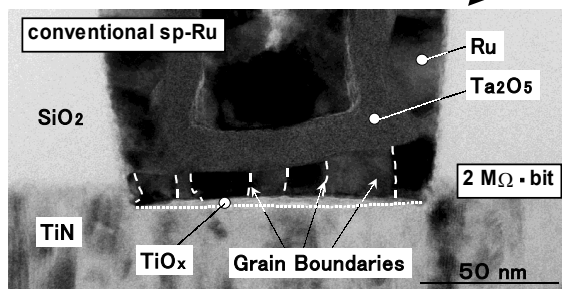


Fig. 5 TEM view of Ru/TiN contact fabricated by using conventional sp-Ru.

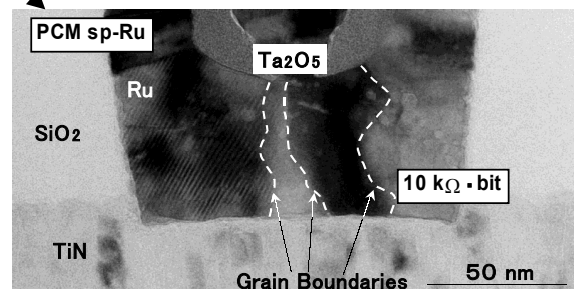


Fig. 6 TEM view of Ru/TiN contact fabricated by using PCM sp-Ru.

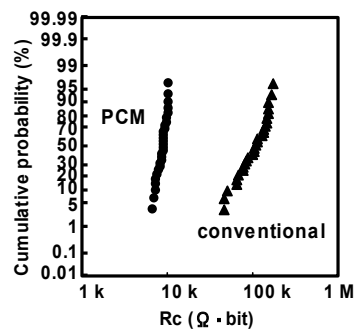


Fig. 4 Distribution of contact resistance of Ru/TiN. Ru thickness was 10 nm.

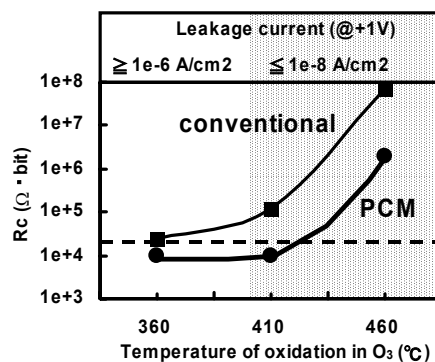


Fig. 8 Contact resistance of Ru/TiN as function of Ta_2O_5 oxidation temperature. Top column shows leakage current of MIM-TaO capacitor.

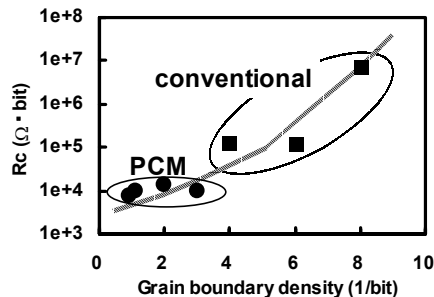


Fig. 7 Contact resistance of Ru / TiN as function of Ru grain boundary density.

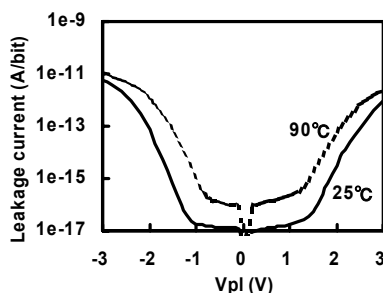


Fig. 11 I-V characteristics of MIM-Ru / TaO / Ru concave-type capacitor.

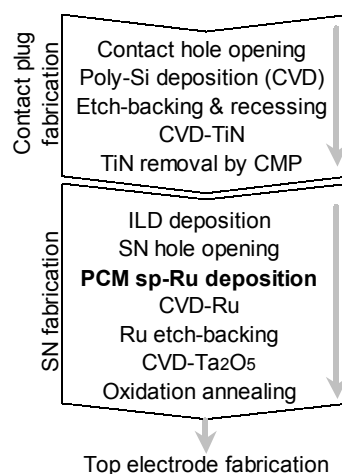


Fig. 9 Process flow to fabricate MIM-Ru / TaO / Ru / TiN / poly-Si capacitor.

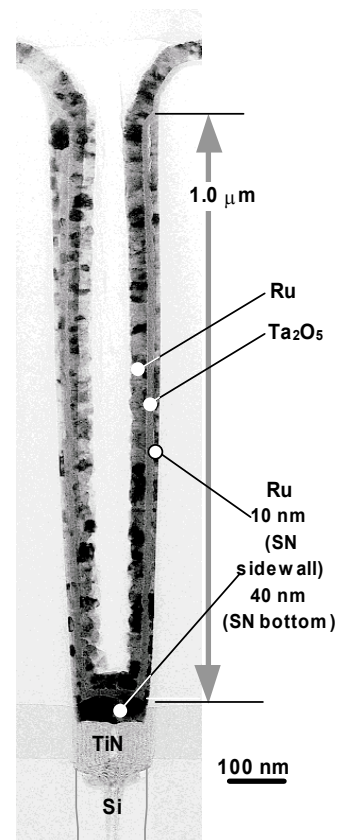


Fig. 10 Cross-sectional TEM view of MIM-TaO capacitor.