Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 248-249

C-5-1 (Invited)

Stress Migration Phenomena of Cu interconnects

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1. Introduction

Stress migration (SM) phenomena in multi-level Cu interconnects are causing serious problems no less than electromigration (EM) or time dependent dielectric break down (TDDB). The SM phenomena are observed as an increase in via resistance caused by void formation in the Cu wiring due to thermal stress. The stress-induced voiding that occurs at process temperatures around 400° C has already been described previously [1]. However, recent reports have shown that degradation can occur at temperatures below 300° C [2,3].

In this study, we investigated SM phenomena for 130-nm-node Cu interconnects [4], and we classified them into two modes: (A) voiding inside vias and (B) voiding under vias. We also discussed the mechanism of the SM phenomena. As a result, we have shown that both modes can be suppressed by the process improvements.

2. Experimental and Discussion

A. Stress-induced voiding inside vias

Figure 1 shows the failure rate of via-chain resistance shifts after baking. The baking was performed at 250° C for 100 hrs without electrical bias. The resistance shift is the difference in the via-chain resistance before and after baking. The five via-chain types were evaluated. Their upper and lower wires have different wire width (0.18 μm, 1 μm, and 4 μm). It was clearly demonstrated that the failure rate of the via-chain resistance strongly depends on the wire width, and wires wider than 1 μm increase the failure rate. This phenomenon was only observed for vias with wide wires above.

Figure 2 is an SEM image of a via failed through 250° C baking. A void appears at the bottom of the via. We also detected carbon on the void wall, which we assumed to be polymer residue. From these results, we considered that the poor adhesion due to locally deteriorated coverage of barrier metal was the main cause of this type of stress-induced voiding, and the degradation mode was accelerated by stress from the wide wires above the vias. Therefore, we optimized both (1) the via cleaning processes to remove the polymer residue and (2) the dry etching processes to improve the via shape. Optimizing these processes enabled completely suppressing this SM mode as shown in Fig. 3.

B. Stress-induced voiding under vias

Although the resistance shift at temperatures above 250°C was suppressed by the process optimizations, another SM phenomenon was observed at stress temperatures below 200° C [2]. Figure 4 shows the failure rate of via chain resistance shift after baking at 175° C for 140 hrs. In this case, a significant resistance shift was observed for the vias with wide wire underneath. This SM mode is enhanced when the line width exceeds 2μm and the temperature range between 150-200° C as shown in Fig. 5.

A cross-sectional TEM image of a via failed through 200° C/140 hrs baking is shown in Fig. 6. A void is visible underneath the barrier metal at the bottom of the via. In our TEM analysis, all voids were connected to Cu grain boundaries.

Figure 7 shows the cumulative probability of the shift of a single-via resistance measured by using four-wire Kelvin measurements. The wire under the via was 5 μm wide. A resistance shift only occurred for 20-30% of the vias, and the rate was independent of the baking time. We consider that one factor determining that a via is “weak” is the distance from the vias to the Cu grain boundaries.

From these results, we explain the mechanism of this SM mode as follows. The driving force of the void formation is the volume contraction of Cu. This driving force increases as the wire width increases. Furthermore, the force increases as the stress temperature decreases. On the other hand, the voiding is caused by the thermal diffusion of vacancies, and the vacancy diffusion is enhanced as the temperature increases. Therefore, the temperature dependence of the failure rate (Fig. 5 (b)) depends on the balance between the driving force and the vacancy diffusion.

We consider that one main diffusion path of the vacancies is the grain boundaries; therefore, the stress migration occurs at vias with grain boundaries underneath or close to them. The vacancies concentrate beneath the via bottom since the stress concentration occurs due to the structural discontinuity at the via bottom.

From this point of view, we focused on the following subjects. (1) Increasing the Cu grain size, (2) decreasing the Cu stress, and (3) improving the adhesion between the barrier metal and the lower-layer Cu at the via bottom. For the subjects, we optimized the annealing conditions after ECP to increase the grain size and performed stress-relaxation treatment to reduce the Cu stress. Furthermore, we used the ionized metal bias sputtering method (IMBS) to improve the adhesion between the barrier metal and the lower-layer Cu [5].

As a result of the above improvements, this mode of SM phenomenon was suppressed at 200° C for over 1000 hrs, as shown in Fig. 8.

3. Conclusions

We studied SM phenomena of Cu interconnects at temperatures below 250° C. We investigated two SM phenomenon modes and found that one mode occurs in vias with wide wires above, and that it could be suppressed by optimizing the via shape and the via-cleaning processes. The other mode occurs under vias with wide wires underneath them. The second mode was suppressed by increasing the Cu grain size, reducing the Cu stress, and improving the adhesion of the barrier metal to Cu.

References

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[3] T. Oshima, et al., Proc. of IEDM2002 pp. 123-126 (2002).
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[5] K.Ishikawa, et al., Proc. of IITC2003 in printing.

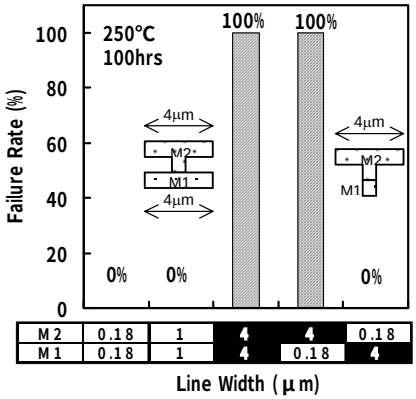


Fig. 1 Dependence of failure rate of via-chain resistance on the line width.

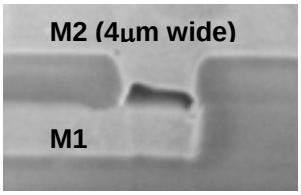


Fig. 2 SEM image of a via failed through 250° C baking

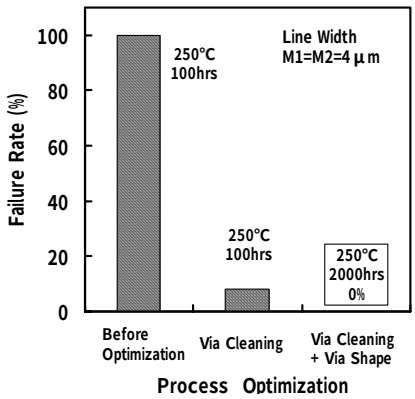


Fig. 3 Failure rate of via-chain resistance shift and process optimization.

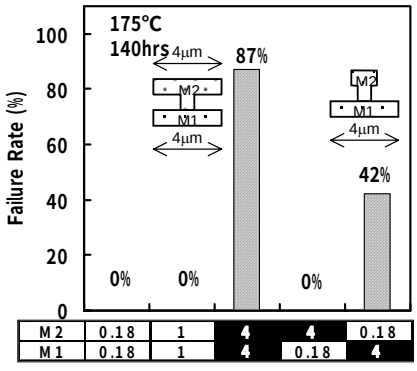
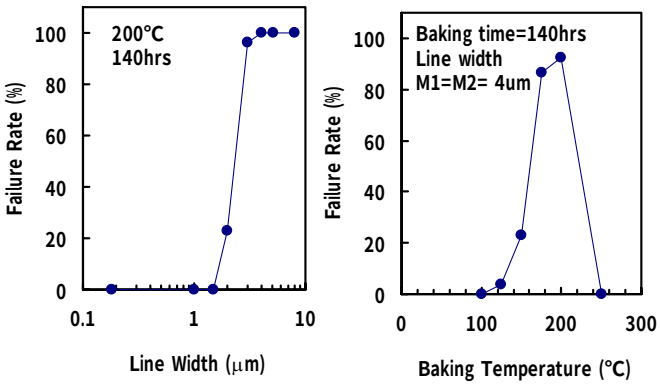


Fig. 4 Dependence of failure rate of via-chain resistance on the line width.



(a) (b)

Fig. 5 Dependence of the failure rate on the line width and the baking temperature.

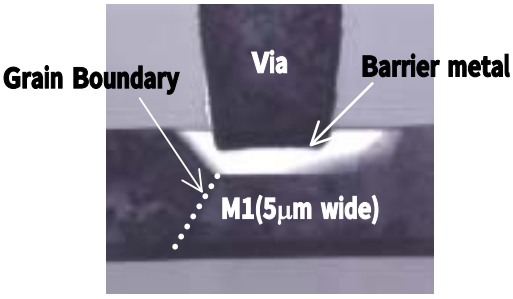


Fig. 6 Cross sectional SEM image of a failed via.

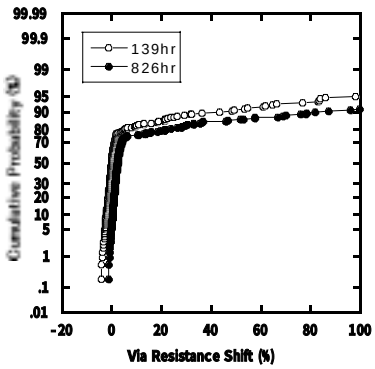


Fig. 7 Cumulative probability of the single-via resistance shift. The baking temperature was 200° C.

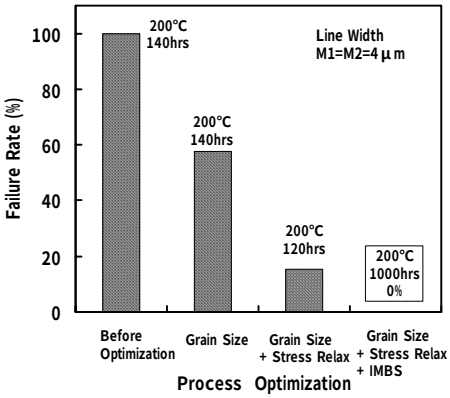


Fig. 8 Failure rate of via-chain resistance shift and process optimization.