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Thin film transistors with oriented cupper phthalocyanine micro-crystals fabricated by physical vapor deposition under DC electric field

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1. Introduction

Thin film transistors (TFT) of organic molecular materials are the promising applicants of next-generation electronic devices. The main targets for present organic electronic devices are the achievement of higher current density and the high-speed operation. Carrier mobility of organic materials is very low compared with Si or other inorganic materials because of the weak interaction between neighboring molecules. In addition, organic TFTs deposited by the standard evaporation method are polycrystalline and often include certain amount of impurities. Though the control of crystallinity and orientation by applying electric field during the deposition had been carried out[1,2], they succeeded in sub-micrometer scale order of cupper phthalocyanine (CuPc) crystals. Considering the electronic device application, micrometer-scale ordering of crystalline films or direct connection of source and drain electrode by single crystals along high conductive axis is favorable. Physical vapor deposition under quasi-thermal equilibrium condition has advantage of making high purity and crystalline films. In addition, the control of crystal orientation is possible with applying DC electric field during the deposition.

2. Experimental

Micro-crystalline film devices were fabricated on 300 nm thick SiO_2 which is thermally grown on heavily doped n-type Si wafer. 20 μm spaced parallel source/drain electrodes and a ring-shaped guard electrode of gold were deposited on the SiO_2/Si wafer by the standard evaporation method. The substrate was placed in the linear cylindrical furnace. The cylindrical furnace is equipped with two heater and N_2 gas flow system whose basic composition is almost the same with that reported by Laudise et al.[3] though minor part has been changed for our purpose. The source temperatures, thermal gradient along cylindrical axis, flux of N_2 gas, and deposition time are experimental parameters. The source material of 95% purity CuPc was purchased from Tokyo Kasei Kogyo Co., Ltd. The maximum temperature of our experimental condition is 550 °C in the gas-preheating zone. The source temperature is about 440 °C, which is controlled by primary heater. The secondly heater tune the temperature gradient along material flow path, cylindrical axis of furnace. The advantage of this method is that CuPc micro-crystals grow under quasi-thermal equilibrium condition. Physical vapor growth of CuPc crystals was carried out under DC electric field of 0 ~ 2.5 MV/m in average between parallel source/drain electrodes with optimized temperature gradient and N_2 flow of 1.2 *l*/min. Substrate temperature was about 200 ~ 320 °C though it was hard to distinguish accurately because of steep temperature gradient. The drain current was monitored during the deposition of CuPc.

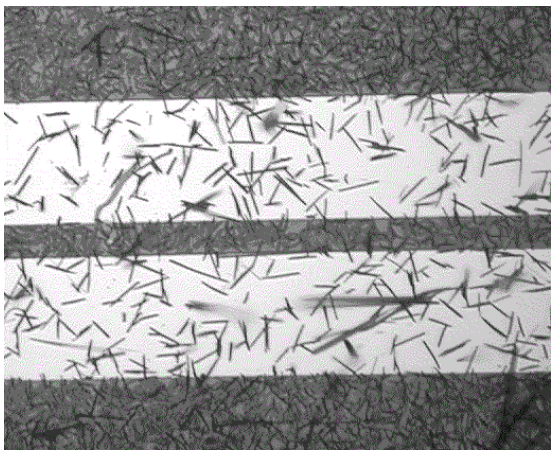

Fig.1 An optical microscope image of a CuPc crystalline film deposited in high temperature area of cylindrical furnace without electric field. The separation of parallel gold electrodes, brighter parts, is 20 μm.

3. Results and Discussion

Figure 1 shows the optical microscopic image of a CuPc crystalline film deposited in 290 ± 20 °C area (high

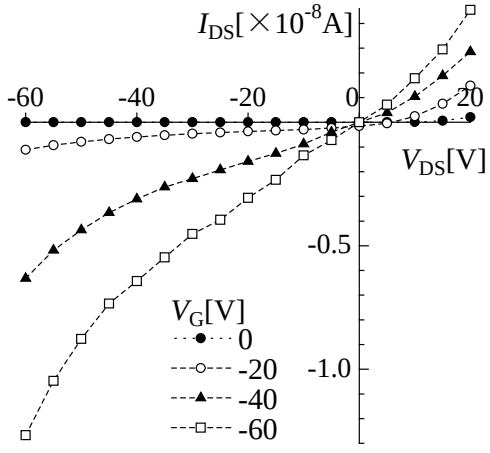

Fig.2 FET characteristics of the CuPc crystalline film shown in Fig.1.

temperature area) in the cylindrical furnace. A pair of horizontal gold electrodes is seen in the center of the image. The dark area around electrodes is the SiO_2/Si substrate surface almost fully covered with CuPc microcrystalline film. The average length of crystal is about 20μm and ~ 2μm width. The crystal coverage on the gold electrode is lower than that on the SiO_2/Si surface.

Fig.2 is the FET characteristics of the crystalline CuPc film shown in Fig.1. P-channel FET characteristics are clearly seen. The field effect mobility of this sample is ~ 1×10^{-4} $cm^2/V\cdot s$ and ON/OFF ratio is over 10^4. High ON/OFF ratio is the evidence of high purity, which is the advantage of the physical vapor growth method. The estimated mobility of the film is lower than that reported by Bao et al. [4], probably be due to the difficulty of channel width estimation. Because the sample consists of the finite set of CuPc micro-crystals, there is frequent discontinuity of a channel and blank spaces on the sample surface. We could not see clear effect of electric field on the morphology of CuPc films deposited in the high temperature area.

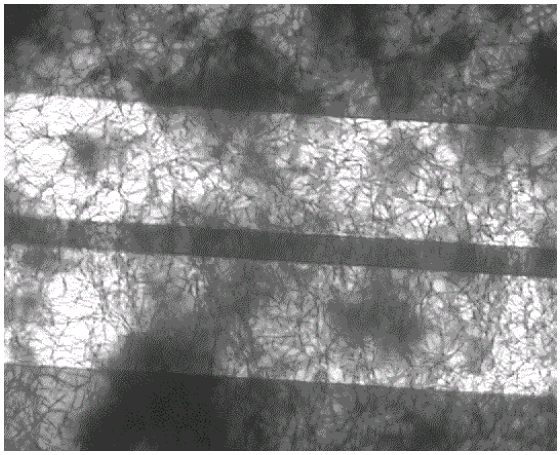

Fig.3 An optical microscope image of a CuPc film in the low temperature area with applied electric field of 0.5 MV/m.

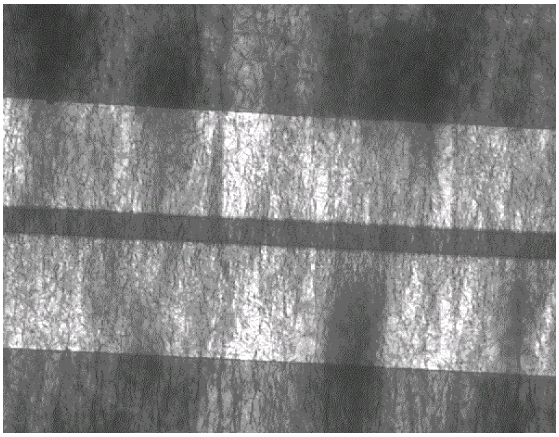

Fig.4 An optical microscope image of a CuPc film in the low temperature area with applied electric field of 1.75 MV/m.

Figure 3 shows an optical microscope image of a CuPc crystalline film deposited in 240 ± 20 °C area (low temperature area) of the furnace. 0.5 MV/m electric field was applied between source and drain electrodes during deposition while the gate electrode remained floated. SiO_2 surface is covered with CuPc micro-crystals while few crystals are distributed on the gold electrodes. Cloud-like structure is seen whole of the picture, which is out of plane growth of CuPc micro-crystals. These crystals are randomly grown in this field strength. Figure 4 is an optical microscope image of the sample with 1.75 MV/m electric field in the low temperature area. From the micrometer-scale view of this sample, we can see the arrangement of crystal row which is almost parallel to the electric field. Conductivity along *b*-axis of CuPc α- and β-phase crystal is higher than that of *a*- or *c*- axis because of efficient overlap of π orbitals between nearest neighboring CuPc molecules.

The difference between the samples deposited in high and low temperature area is mainly due to the molecular flux and diffusion activity. If the growth speed is sufficiently low and diffusion of molecules is high, nuclei oriented to the direction stabilized by the external electric field will survive and keep growing while other nuclei will diminish. Because high temperature area is upper course of cylindrical furnace, excessive molecular flux is supplied on the substrate. In addition, it is known that the transition temperature of β- and α-phase is around 200 °C, which is possibly another reason for the difference between high and low temperature condition. Although the selective growth of crystal is difficult in this condition reported here, by optimizing the growth condition, it should be possible to achieve orientation-control of larger crystals even in the high temperature area.

4. Conclusions

We successfully fabricated the crystalline CuPc films by physical vapor deposition using the cylindrical furnace. Micrometer-scale ordering of CuPc crystalline film was obtained by optimizing deposition condition and electric field strength.

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