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Conductive Atomic Force Microscopy Analysis for Local Electrical Characteristics in Stressed SiO_2 Gate Films

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1. Introduction

It is well known that stress-induced leakage current (SILC) is induced in the gate oxide films by applying the high electric filed. The percolation theory [1] provides one of useful models for explaining the occurrence of SILC, where defects with a nanometer scale generated locally in the gate oxide films are origin of the leakage current.

Conductive atomic force microscope (C-AFM) is a powerful tool to measure nanometer scale electrical characteristics. Recently, Porti *et al* [2] demonstrated the capabilities of this method to measure the local electrical characteristics of SiO_2 gate films. However, there are few studies for intentionally-stressed gate oxides in the actual device systems. In particular, the relationship between macroscopic characteristics and microscopic electric properties of the systems has not been clarified yet.

In this work, we performed nanometer scale observations for local current leakage sites in the stressed SiO_2 gate films using C-AFM and successfully detected the current leakage sites which are the origin for SILC observed in the macroscopic measurement.

2. Experimental

The devices used in this experiment have a metal-oxide-semiconductor (MOS) capacitor structure with a n^+-polysilicon gate electrode / gate SiO_2 / n-Si substrate. The SiO_2 film with a thickness of 11.3 nm was thermally grown at 900°C in wet ambient. The capacitor area was 4×10^{-4} cm^2. Fowler-Nordheim constant current stress (FN stress) with a current density of 100 mA/cm^2 (gate bias was negative) and a stress time of 100 sec was applied. The current-voltage (I-V) characteristics were measured before and after FN stress. The capacitance-voltage (C-V) characteristics were also measured before and after FN stress to analyze the nature of trapped charges in the gate SiO_2. For C-AFM measurements for the devices after FN stress, the n^+-polysilicon gate material was firstly removed using TMAH [3] at 60°C. Then, the gate SiO_2 was thinned by diluted HF (0.1%) at room temperature to a thickness of 5.2 nm which was confirmed by elipsometry. The C-AFM was performed using JEOL JSPM-4200 which was originally modified to realize the detection of small currents of 0.01 pA range. Surface topography and current images were simultaneously obtained by C-AFM at room temperature in air ambient. In the current image, a leakage spot was identified as a site where the current exceeded a threshold value which was defined from the mean value and the standard deviation of currents in the scanned area.

3. Results and Discussion

Figure 1 shows macroscopic electrical characteristics of the SiO_2 gate films in the actual devices. Large SILC was observed in the I-V curve for the stressed sample. Inset shows simultaneously-measured C-V characteristic for the same sample. Compared with the curve for a non-stressed sample, a large shift to a negative voltage was clearly observed. This shift indicates that holes were trapped in the film due to FN stress. On the other hand, these holes were detrapped when the I-V measurement was repeated. In this case, SILC was observed to decrease.

Figure 2 shows a C-AFM image of the non-stressed sample taken at $V_{sub}= -6$ V. In the image, no current spots were observed. On the contrary, leakage current spots were clearly observed in the stressed sample, as shown in Fig. 3. A mean value of currents for the observed spots was 0.52 pA at $V_{sub}= -6$ V. When assuming that these current spots were caused by local thinning of the SiO_2 films, the thickness reduction was estimated to be 0.36 nm. On the other hand, root-mean-square of surface roughness was measured to be 0.29 nm. Thus, the observed current spots do not come from the thickness fluctuation of SiO_2 but explicitly reflect leakage sites which locally generated in the film by FN stress. Moreover, we estimated SiO_2 thickness fluctuation to be 0.16 nm using a background current fluctuation of 0.1 pA. This value was smaller than the observed surface roughness of the SiO_2 film.

Figure 4 shows a current image of the sample in which holes were confirmed to be detrapped due to the repeated I-V measurement shown in Fig. 1. No current spots were observed. However, when applying a higher voltage up to –7 V to take a current image, spots appear again, as seen in Fig. 5.

Figure 6 shows applied voltage dependencies of the number of observable spots and the mean current of the spots when taking current images. Comparison between two samples in which holes are trapped and detrapped, there is a critical difference of a threshold voltage at which the spots start to appear. Furthermore, in both samples, the number of spots initially increases with the voltage to a certain value, then decrease. On the other hand, the spot current was increased with an increase in the applied voltage. The observed positive voltage shift between two samples is about 1 V at 0.5 pA. This value is closely related to a positive voltage shift of about 2 V appeared in the C-V

curve of the hole-detrapped sample shown in the inset of Fig. 1: the SiO_2 film thickness in this sample observed by C-AFM was about a half of that for the macroscopic C-V measurement. These characteristics indicate that at least two types of defects causing the current spots exist in the stressed SiO_2 films: one at which the leakage current is enhanced and the other at which the current is diminished with the applied voltage.

4. Conclusions

We have investigated the FN stressed SiO_2 gate films using C-AFM. The leakage current spots were successfully observed in the samples where the SILC was confirmed by the macroscopic measurement. This leakage current spots were caused by the defects in the stressed SiO_2. From voltage dependence of the appearance and the current of the spot, we found that at least two types of defects were generated due to FN stress.

References

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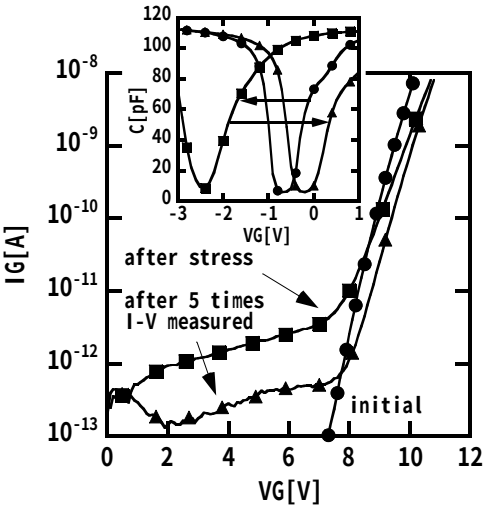
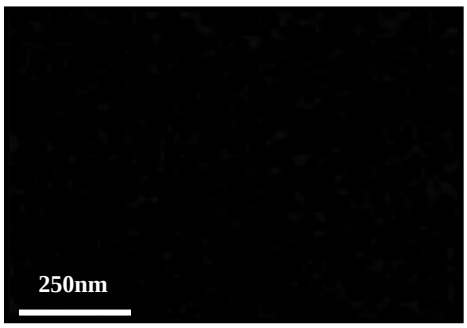


Fig. 1 Results of macroscopic I-V and C-V (inset) measurements for the MOS capacitors under various stress conditions.



F ig. 2 Current image of a non-stressed sample taken at a sample voltage of –6 V.

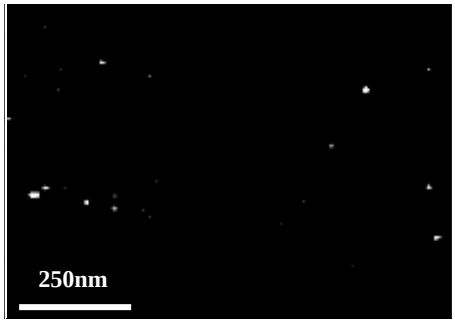


Fig. 3 Current image of a stressed sample taken at a sample voltage of –6 V. A mean current from the spots was 0.52pA.

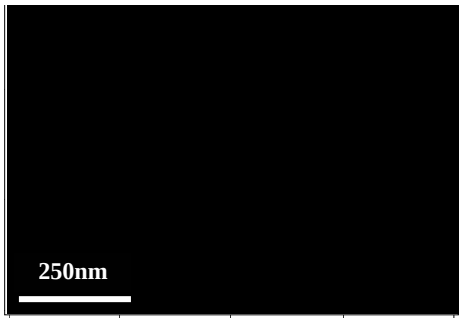


Fig. 4 Current image of a hole-detrapped sample taken at a sample voltage of –6 V.

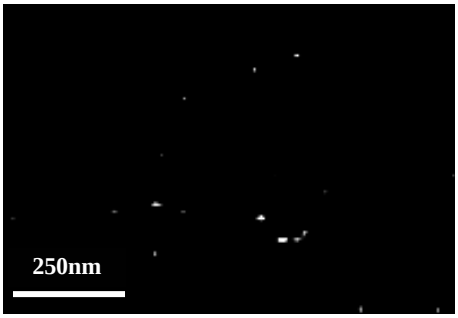


Fig. 5 Current image of a hole-detrapped sample taken at a sample voltage of –7 V. A mean current from the spots was 0.65 pA.

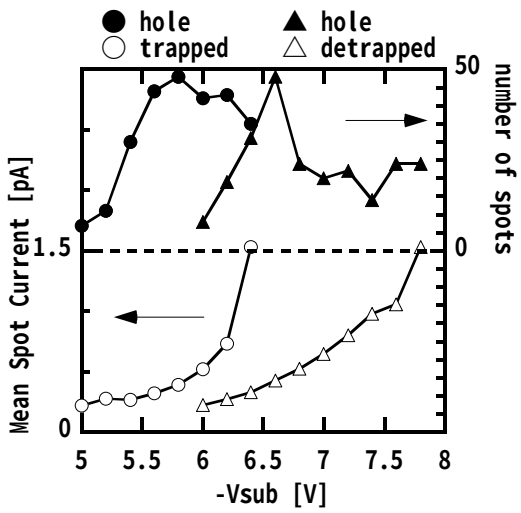


Fig. 6 Voltage dependence of mean currents from the spots and the number of spots. Two samples in which holes are trapped and detrapped are compared.