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Selective Dry Etching of HfO_2 in CF_4, Cl_2 and HBr Based Chemistry

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1. Introduction

High-k gate dielectrics have been investigated for low power CMOS applications in the 65 nm technology node and beyond. Among several candidates, HfO_2 is being extensively studied because of its modest dielectric constant and thermal stability at the interface with Si [1, 2]. To integrate HfO_2 with conventional CMOS processes, a controllable patterning process of the etch resistant film is essential. In particular, selective etching to remove HfO_2 on SiO_2/Si is extremely important in order to maintain the controllable formation of shallow junctions. There have been reports of high-k etching using BCl_3/Cl_2 based plasma [3] or with a combination of oxygen plasma and subsequent DHF treatment [4]. However, the highly selective etch of HfO_2 on SiO_2, with the damaged layer removable in subsequent wet etch step, has not yet been achieved satisfactorily. In this study, we investigated HfO_2 etching characteristics in conventional Si gate etching chemistries, in which a low SiO_2 etching rate is easily obtained, thus achieving the required HfO_2 : SiO_2 selectivity. CF_4 is expected to reduce HfO_2, while Hf- chloride or bromide have relatively high vapor pressure, therefore these chemistries are expected to etch HfO_2. Moreover, the etchability of dry-etched HfO_2 using a wet treatment was also investigated.

2. Experiments

HfO_2 films (3 - 7 nm) were deposited by Atomic Layer Deposition (ALD) onto 1-nm thick SiO_2 interfacial layers formed by In-Situ Steam Generation (ISSG) on 300 mm Si wafers. Films were then annealed at 800°C for 5 s, followed by 150-nm thick poly-Si deposition. After P^+ ion implantation, TEOS masks were fabricated for gate patterning.

Poly-Si gates were etched in a conventional Si etch system with an Inductively Coupled Plasma (ICP) source. HfO_2 films were then etched subsequently in the same chamber with a two-step process (a main etch step (a): CF_4 and an etch completion step (b): $Cl_2/HBr/O_2$ chemistries).

After ashing the etch by-product, samples were spin-etched in dilute HF (DHF).

Film thicknesses were measured using X-ray Fluorescence (XRF) for blanket or ellipsometry for patterned samples. Etch profiles were examined by cross sectional Scanning Electron Microscope (SEM).

3. Results and Discussion

Wet etching of previously dry-etched HfO_2

Figure 1 shows the etched depth by dry etching using steps (a) and (b) as a function of time for HfO_2 blanket wafers. HfO_2 etching in CF_4 was assisted by the high ion and/or neutral density in the ICP discharge, even though Hf-fluoride has relatively low vapor pressure. The depths after a subsequent 30 s DHF etch were also plotted. The layer thicknesses removed in the wet etching step were almost independent of dry etch time in the range examined in this study.

Figure 2 indicates the layer thickness removed in wet etching step as a function of time for HfO_2 blanket wafers which had been subjected to two minutes of a dry etch step of either type (a) or (b). Etching stopped after approximately 2 minutes at about 0.6 nm. These layers may be regarded as the plasma damaged layers remaining after dry etching. The depth of plasma damage under our dry etching conditions is considered to be in the range of several nm [5]. Only highly damaged layers were thought to be etched away in the wet etch step because the damaged layer thickness removed in our experiments was smaller than expected.

Etching rate of HfO_2 for a patterned sample

We performed the same experiments for patterned samples as Fig. 1 and defined the etch rate as the slopes of depths after DHF etching. Figure 3 shows the HfO_2 etch rates for step (a) and (b), co-plotted with Si and SiO_2 etch rates. The etch rates for patterned samples were higher than those for blanket samples. The mechanism for this etch rate enhancement is under investigation. Adequate etch rates of 2.0 nm/min were obtained for patterned samples using either etch steps (a) or (b). A selectivity of 1.9 over underlying SiO_2 was obtained for step (b).

Patterning of poly-Si/HfO_2 stacks

We selected etch step times to permit complete etching of the HfO_2 layers, whilst suppressing both the loss of TEOS mask in step (a) and the formation of the HfO_2 tapered feature at the bottom of the gate in step (b). Moreover, we optimized step (b) to improve the uniformity of etch rate and to suppress HfO_2 tapered feature. Satisfactorily etched surfaces were obtained over a whole 300 mm wafer without any HfO_2 residue nor etch-pitting as shown in Fig. 4. The HfO_2 tapered feature is considered to be caused by side etching of poly-Si gate and/or foot formation by the deposition of etch by-product at the

bottom of the gate. It became more pronounced as the HfO_2 etch time was extended. This feature needs further suppression, though the situation would be less serious at the final target thickness of less than 3 nm.

Using the etching process developed in this study, a MOSFET with HfO_2 as gate dielectric was successfully fabricated as shown in Fig. 5.

4. Conclusions

Using CF_4, Cl_2, HBr based chemistries, we obtained an adequate rate of etch and selectivity of 2.0 nm/min and 1.9, respectively. Moreover, it was clarified that the top portion of the highly damaged layer created by HfO_2 dry etch step can be removed by a subsequent wet etching. Based on these results, patterning of poly-Si/HfO_2 gate stacks were successfully demonstrated.

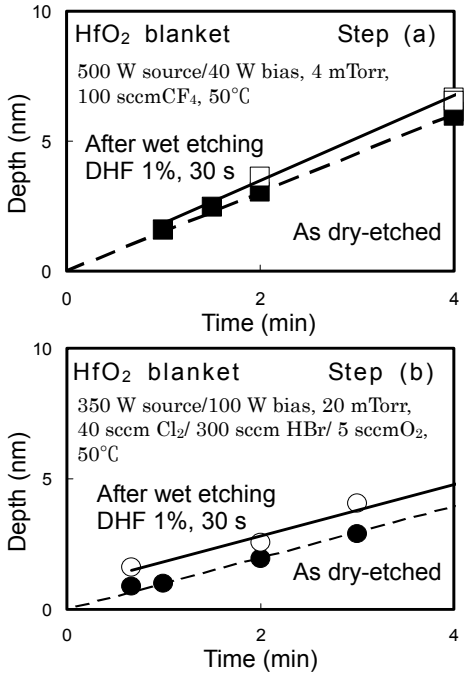

Fig. 1 Etched depths by dry etching using step (a) and (b) as a function of dry etching time for HfO_2 blanket wafers. Depths after wet etching are also plotted.

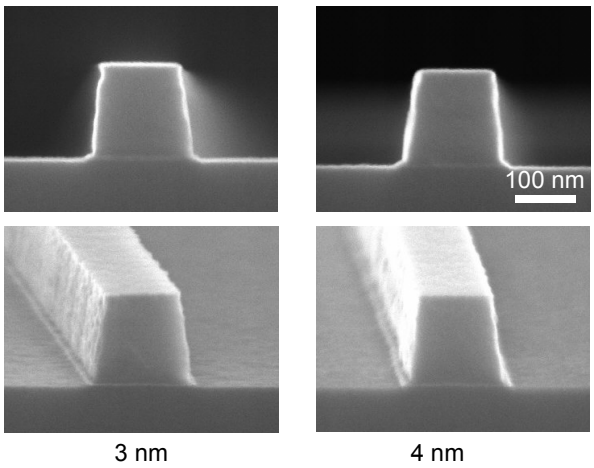

Fig. 4 Etch profiles for 3 nm and 4 nm HfO_2 patterned wafers.

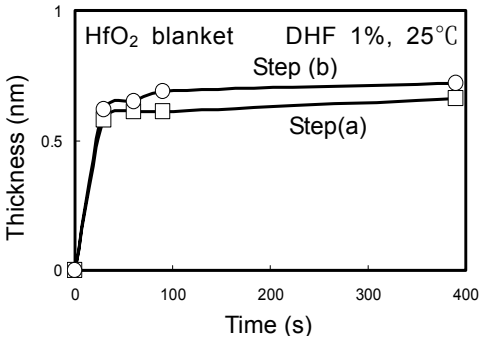

Fig. 2 Removed layer thickness in the wet etching step as a function of wet etching time for HfO_2 blanket wafers preceded by two minutes of dry etching using step (a) or (b).

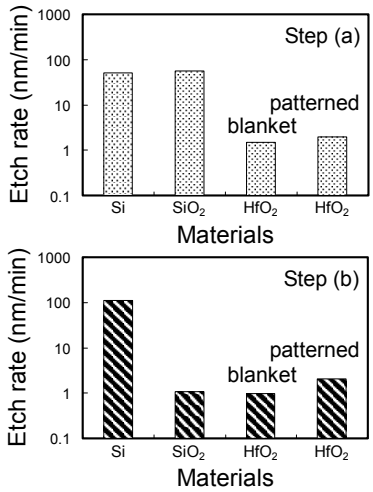

Fig. 3 HfO_2 etch rates for step (a) and (b) co-plotted with Si and SiO_2 etch rates.

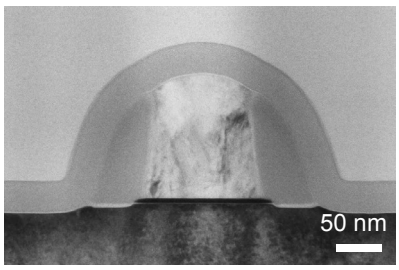

Fig. 5 Cross sectional TEM image of a MOSFET with 4 nm HfO_2 gate dielectric.

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