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Impact of NiSi Thermal Instability on Junction Shallowing Characterized with Damage-free n+/p Silicon Diodes

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1. Introduction

Based on the ITRS roadmap, the 90nm node MOSFET technology demands deep S/D junction depth, x_j, shallower than 75nm. At the same time, for sheet resistance reduction, application of silicide on the S/D is a necessity. For this purpose, $CoSi_2$ is a common choice. Recently, however, it has been revealed that a substantial Co in-diffusion and resultant GR center formation are intractable sources of severe junction leakage inherent to Co silicidation[1]. To circumvent this difficulty, growing attention is now directed to NiSi as an alternative silicide material. For leakage suppression, smaller Si consumption and lower formation temperature of NiSi are thought to be great advantages over $CoSi_2$ [2]. Nevertheless, NiSi is not a problem-free option. Actually, thermal instability of a thin NiSi film is a primary concern. In fact, the film's thermal stability is customarily monitored with resistivity changes caused by annealing[2,3]. Notably, however, its impacts on junction leakage, i.e., NiSi's foremost advantage, have never been studied in a coordinated manner. Moreover, the origin of the NiSi junction leakage is not yet fully understood. Although silicide spikes and interfacial asperity are sometimes blamed[4], a true profile of the leakage generator is still elusive. Therefore, technologically, clarification of a practical limitation on the junction shallowing imposed by NiSi thermal instability is urgently required. Also, scientifically, identification of a principal leakage mechanism is highly desirable. Thus, the present paper reports a basic and systematic study of annealing effects on NiSi junction leakage.

2. NiSi Formation on Damage-Free Junction

Fig.1 illustrates the procedure for damage-free junction formation employed in this study. The details of the fabrication will be found in ref. [1]. After formation of a virtually flat p-well of $2x10^{17}cm^{-3}$ concentration, a junction region is delineated by RIE-etching a SiN film and wet-etching an underlying TEOS film, avoiding plasma damage to the substrate (Fig.1-a). Subsequently, AsSG film is deposited and annealed to form an n+ region by solid phase diffusion into the opening defined above (Fig.1-b). By adjusting the annealing time and temperature, n+/p junctions with various depths can be readily obtained[1]. After AsSG removal by wet etching, a pad TEOS layer and a SiN film are applied. The following SiN RIE stops at the pad TEOS and leaves sidewalls to guard the periphery (Fig.1-c). Next, after wet etching the pad TEOS, Ni is sputtered and an ensuing thermal process promotes about 30-nm-thick NiSi formation. Subsequent removal of unreacted metal creates the final junction structure (Fig.1-d). Because the n+ region extends outside the stuffing sidewall and the NiSi formation is well contained within the n+ region, these junctions are free from any anomalous leakage at their perimeters. Furthermore, absence of heavy implantation damage enables these junctions to illuminate intrinsic properties of the NiSi film.

3. Leakage Generation by Post-Annealing

In order to assess the impact of thermal processing on junction leakage, the above junctions were post-annealed in N_2 at around silicidation temperature (T_S) for up to 90min. Fig.2 plots leakage levels (I_R at V_R=4V) as a function of the junction depth for each post-anneal condition as specified in Table I. At T_L, no leakage generation was observed down to x_j=61nm. A sudden increase in leakage at the shallowest depth (x_j=51nm) is almost independent of the annealing time. At T_S, additional leakage at deeper depths and a small but unmistakable ingressive movement are already in evidence. At T_H, measurable leakage generation and a sizeable inward migration are clearly visible. Fig. 3 is the Weibull plot over 312 junctions after 90min annealing for each temperature and depth. Strikingly, regardless of the annealing conditions, the thermally induced leakage keeps tight ensemble distribution. Absence of large deviation negates the presence of a sporadic and destructive leakage generator such as a silicide spike even at 21nm below NiSi (i.e., x_j=51nm). Furthermore, activation energies (Ea's) of the leakage currents are found to be around the mid-gap, as demonstrated in Fig.4. These facts strongly suggest numerous formations of GR centers during the annealing near the Si mid-gap. In order to further assess the nature of the GR centers, Ea's are plotted as a function of I_R in Fig. 5. Unlike data scattering in Fig.4, with the increase of the annealing temperature, Ea's start to be unified into a single characteristic curve that is distinctly embodied by the T_H data. To shed deeper light on the meaning of the convergence, Ni SIMS data measured from the backside of the substrate were correlated with the leakage-depth profiles. The excellent matching shown in Fig.6 provides direct evidence of Ni involvement in the GR center formation. Now, because I_R is shown to be a function of Ni concentration (C_{Ni}), Ea convergence with I_R indicates stable GR center formation as a function of C_{Ni}. And the gradual change of the characteristic curve with I_R can be explained by continuous structural evolution of some complex defects, stimulated by varying C_{Ni} and forming a defect-band, rather than abrupt transition between discrete energy levels of specific point defects. In fact, the excellent matching in Fig.6 also allows a rough estimate of the leakage per Ni atom. An effective cross-section of $2.0x10^{-14}$ cm^2 comes about. This is much larger than that expected from atomic Ni (i.e., less than 10^{-16} cm^2 [5]). Thus, it is highly likely that the thermally induced GR centers are the result of clustering of Ni atoms released from the NiSi layer during the annealing. This leakage mechanism is illustrated in Fig.7. Another distinguishing feature of Fig.6 is its peculiar migration kinematics. Fig.8 plots squares of leakage depths (at $I_R=10^{-7}A/cm^2$) as a function of annealing time. The linear dependency obtained for both T_S and T_H points to a steady diffusion as the governing migration kinematics, although the obtained diffusion coefficient ($62nm^2$/min at T_H) is much smaller than the atomic value ($3x10^6$ nm^2/min[6]). This again corroborates the cluster origin of the GR center. Noticeable also is the fact that the intersections with the y axis are far from the origin, especially for T_H. This fact implies that, at an early stage of the annealing, i.e., before stable diffusion sets in, substantial Ni must have burst into the Si substrate. Fig.9 shows this initial Ni burst as a function of temperature. The initial Ni burst is superimposed over the intrinsic Ni infiltration during silicidation. In effect, Fig.9 demarcates a practical limitation of junction shallowing as a function of the highest process temperature. Clearly, to take full advantage of NiSi, process temperatures should be kept below T_S. With this restriction, an ultra-shallow junction (about 20nm deep below silicide) can be readily achieved by NiSi.

4. Summary and Conclusion

Using n+/p junctions formed by solid phase diffusion, a clear correlation between junction leakage and NiSi thermal instability has been readily established. Clustering of Ni atoms released from the NiSi layer and subsequent GR center formation were identified as a principal leakage mechanism induced by annealing. In addition, these damage-free junctions unveiled a peculiar Ni migration kinematics. Anomalous Ni bursts at the initial stage of annealing imposes a strong restriction on the allowable process temperature.

References

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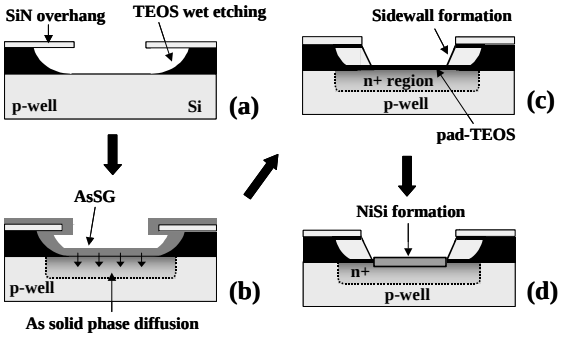

Fig.1 n+/p junction formation procedure to fabricate damage-free diodes. Solid phase diffusion from AsSG is used for creating the n+ region. NiSi formation is well contained within the n+ region.

Post-Anneal Conditions	
T_L = T_s-50°C	30 min.
	60 min.
	90 min.
Ts Silicidation Temperature	30 min.
	60 min.
	90 min.
T_H = T_s+50°C	10 min.
	30 min.
	60 min.
	90 min.

Table I Post-anneal conditions applied to the junctions in Fig.1.

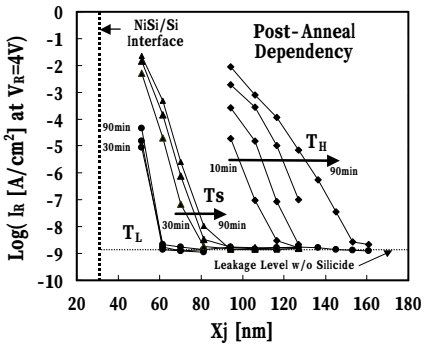

Fig.2 Leakage levels plotted as a function of junction depth for each annealing condition specified in Table I.

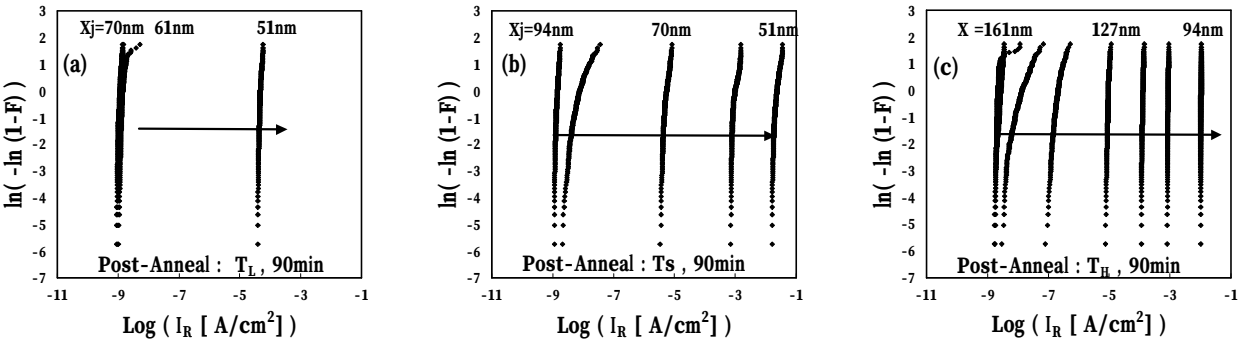

Fig.3 Weibull plot over 312 junctions after 90 min annealing at (a) T_L, (b) Ts, and (c)T_H for various junction depths. Regardless of the annealing conditions, leakage generation proceeds in each and every junction in concert with the reduction of junction depth.

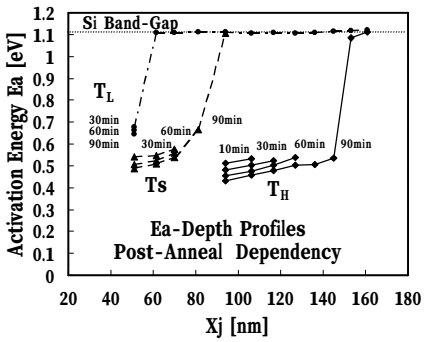

Fig.4 Activation energies of the leakage currents plotted as functions of junction depth for various post-anneal conditions. After the leakage generation, the activation energy sharply drops to near the Si mid-gap level.

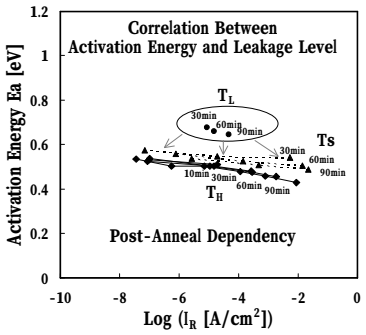

Fig.5 Activation energies plotted as functions of leakage level. Unlike scattering in Fig.4, the activation energies start to be unified into a single characteristic curve with annealing.

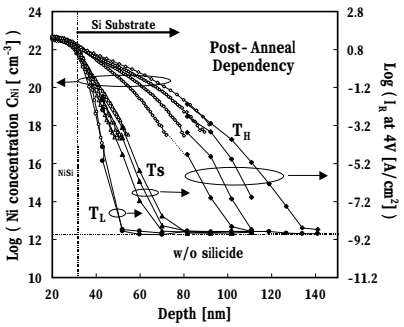

Fig.6 Correlation between Ni Backside SIMS profiles and leakage-depth profiles for various post-anneal conditions. Stretch of depletion layer into n+ region is taken into account.

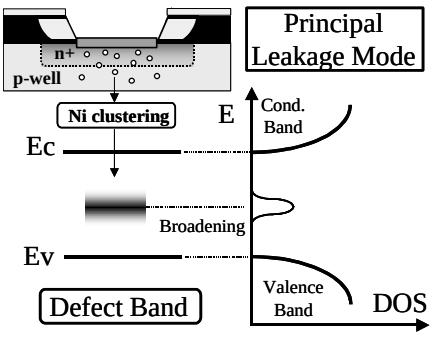

Fig.7 Model of thermally induced junction leakage. Ni atoms released from NiSi layer cluster in Si substrate to form a complex defect. Band-like states are created in the Si gap.

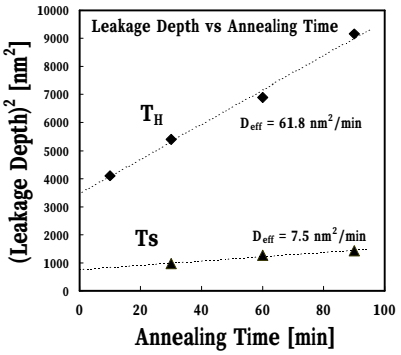

Fig.8 Square of leakage depths plotted as a function of annealing time. GR centers migrate by diffusion mechanism.

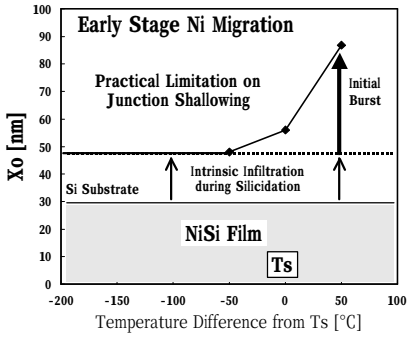

Fig9 Anomalous Ni burst observed at an initial stage of annealing plotted as a function of anneal temperature. Intrinsic Ni infiltration by silicidation is also superimposed.