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Strained Si MOSFETs on SiGe-on-Insulator (SGOI) for High Performance CMOS Technology

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1. Introduction

The semiconductor industry is actively exploring novel device structures and materials that can boost performance of CMOS technology. SOI MOSFETs increase circuit speed with reduction in junction capacitance and by advantage in gate length scaling. Strain enhances carrier transport properties of Si, and various groups have studied and demonstrated strained Si (SS) MOSFETs. (e.g. [1, 2])

The advantages of SOI and strained Si can be combined in MOSFETs fabricated on SiGe-on-insulator (SGOI) as shown in Fig. 1. In addition, some of the disadvantages of strained Si/SiGe system such as larger junction capacitance and leakage are eliminated by the SOI structure. In this paper, demonstration of deep submicron SGOI device is reported, and the challenges in bringing SGOI to mainstream CMOS technology are described.

2. SGOI Device Demonstration

SGOI was fabricated by the "thermal mixing" technique [3] that involves epitaxial growth of SiGe on SOI substrate and thermal treatment to interdiffuse Ge at high temperature. Fig. 2 shows the cross-sectional TEM (XTEM) and plan view TEM (PVTEM) of 20 nm strained Si layer grown on 35 nm thick TMSGOI. The SiGe layer is partially relaxed, very smooth, (0.5 nm roughness.) and contains very few defects. Fig. 3 compares electron mobility measured in long channel devices fabricated on SGOI and SOI. At high carrier concentration, electron mobility is enhanced by over 50%, consistent with the observations in bulk strained Si MOSFETs.

Short channel MOSFETs were fabricated on TMSGOI. Fig. 4 shows the XTEM of a fabricated 60 nm device with 2.3 nm T_{ox} on 55 nm-thick TMSGOI (15 nm Si/40 nm SiGe.) Various fabrication steps in a base-line CMOS technology have been modified to ensure process compatibility with the strained Si/SiGe hetero-layers. For typical ultra-thin gate oxidation conditions, the oxidation rate and gate oxide leakage characteristics were found to be identical to those of unstrained Si. Fig. 5 compares the current drive of SGOI devices to that of SOI devices. In DC measurements, the SGOI devices exhibited ~7% higher current drive. The pulse I-V technique [4] was used to reduce the effect of self-heating in current drive characterization. (Fig. 6) The measurements indicated that self-heating was considerably larger in SGOI due to the lower thermal conductivity in SiGe and ultra-thin Si channel layer. Without self-heating, current drive enhancement in SGOI is significantly larger at ~20%.

SGOI can also be fabricated by the layer transfer technique. [5] Fig. 7(a) shows the XTEM of a 50 nm gate device fabricated on bonded SGOI (BSGOI), which was created by transferring a thin layer of SiGe from an epitaxially grown relaxed SiGe buffer. Another layer of relaxed SiGe and strained Si channel layer were regrown after the layer transfer. Although the technique involves a wafer bonding step, it takes advantage of the graded relaxed SiGe buffer which is a well-understood way to form relaxed SiGe available for layer transfer. Good V_T control was achieved for NFETs with gate length down to 50 nm. Pulse *I-V* measurements (Fig. 7(b)) indicated comparable amount of self-heating and current drive enhancements as in TMSGOI.

3. Challenges in SGOI Technology

In addition to the critical issue of material quality, properties of SiGe have to be carefully taken into account in designing device integration. Low resistivity cobalt silicide formation, for example, is inhibited by SiGe. [6] In this work, raised source/drain structure was formed by selective epitaxy of Si (shown in XTEM in Fig. 4) to provide adequate thickness of Si required for reaction with cobalt. Arsenic diffusion is significantly enhanced in SiGe while boron diffusion is suppressed. Interaction of SiGe with various oxidation and etching steps require modifications in order to maintain the integrity of both the strained Si and SiGe layers. Junction leakage is also affected by the changes in energy gap and doping profile in SiGe, so the floating body effect in SGOI device is expected to be different from that of SOI device. Hole mobility enhancement in high vertical field and inversion carrier density requires large (>1.2%) amount of tensile strain. [6] In order to achieve enhancement of both NFET and PFET mobility, Ge content of >30% is required in fully relaxed SiGe under the strained Si channel. Ultra-thin strained Si can be formed directly on insulator with no SiGe layer present by the layer transfer technique and selective SiGe removal [7]. Such structure (Fig. 8) can extend the advantage of strained Si to ultra-thin body SOI devices without the challenges associated with SiGe.

4. Summary

The advantages of SOI and strained Si have been combined in strained Si MOSFETs on SGOI integrated in a current CMOS technology, demonstrating that it is possible

to boost the performance of future SOI CMOS technology.

Acknowledgments

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References

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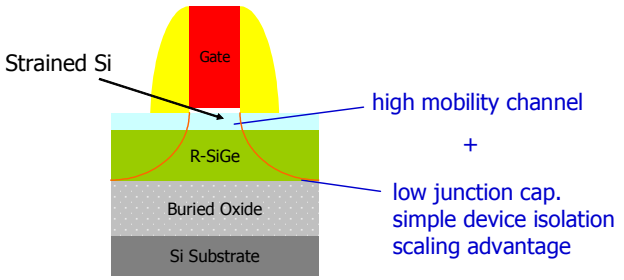

Fig. 1. Strained Si MOSFET on SiGe-on-Insulator (SGOI).

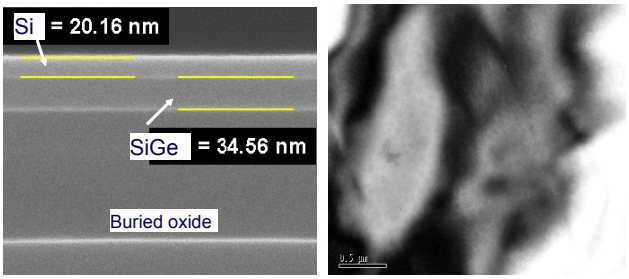

Fig. 2. XTEM and PVTEM of ultra-thin strained Si on TMSGOI.

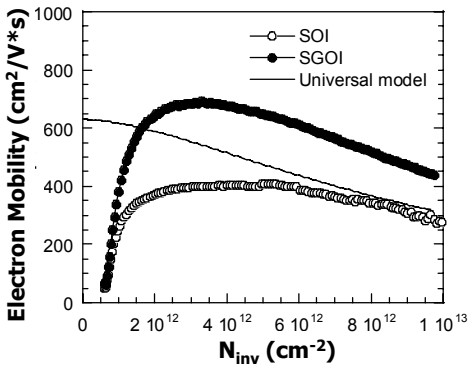

Fig. 3. Electron mobility vs. inversion carrier density. Mobility of SGOI device is enhanced by >50% compared to SOI.

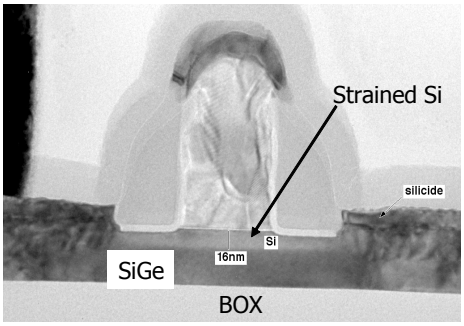

Fig. 4. XTEM of 60 nm MOSFET fabricated on TMSGOI. Raised source/drain was formed by selective epi growth of Si.

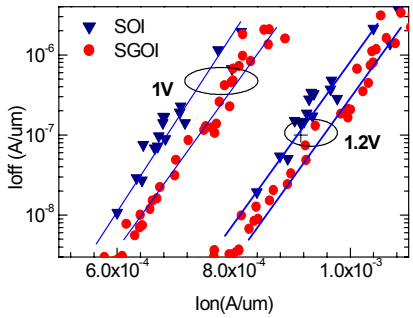

Fig. 5. I_{off} – I_{on} comparison between SOI and TMSGOI NFETs. SGOI NFETs exhibit larger current drive in spite of the larger self-heating expected in SGOI.

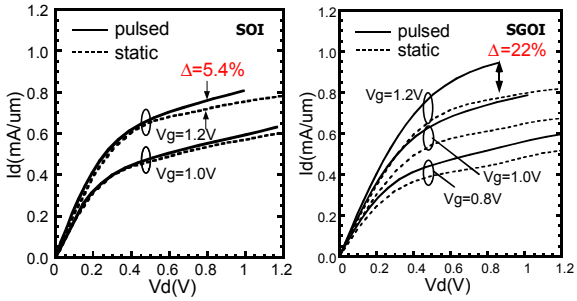

Fig. 6. Comparison of *I-V* measured on a TMSGOI NFET by pulse technique and DC static characterization. SGOI clearly exhibits larger difference between pulse and static measurements.

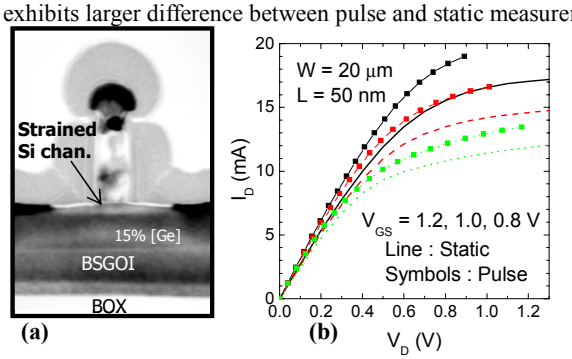

Fig. 7. 50 nm NFET fabricated on BSGOI. (a) XTEM, (b) *I-V* by pulse and static measurements.

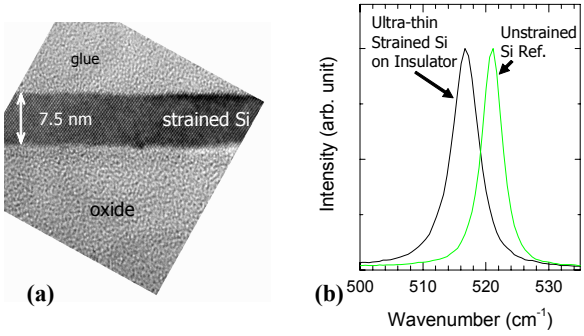

Fig. 8. Strained Si directly on buried oxide fabricated by the layer transfer technique. (a) HR XTEM and (b) Raman analysis showing that the strain in Si is maintained after layer transfer.