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Fabrication of Ultra-Thin Strained Ge-on-Insulator Substrate by Ge-Condensation Technique

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1. Introduction

Improving carrier mobility in metal-oxide-semiconductor field-effect transistors (MOSFETs) is an important issue for improvement of performance of CMOS circuits[1] because of the fundamental limit of scaling. Ge channel have attracted much attention because of high mobility of both electrons and holes. Especially, when the Ge layer is compressively strained, it exhibits a drastic enhancement of hole mobility much higher than that of strained Si[2]. In fact, hole mobility enhancement in a strained Ge channel up to 2700 cm^2/Vs at room temperature was reported recently[3]. Another technique to improve the performance of the CMOS circuits is introducing Si-on-Insulator (SOI) structure because of the low parasitic capacitance. Especially for full-depleted (FD) type SOI structure, reduced SOI thickness is required (less than 10 nm for 65 nm technology node and beyond). By combining these two techniques, we can expect high performance CMOS circuits of strained Ge-on-Insulator (GOI) structure.

In this paper, we report a new fabrication method of an ultra-thin (~10 nm) strained GOI substrate for FD strained GOI-MOSFET, which has advantages of both of high mobility channel and FD SOI structure. We used the Ge-condensation by oxidation technique[4] in our GOI fabrication method, in which a SiGe layer that is grown epitaxially on an SOI wafer is oxidized at a temperature typically higher than 1000°C. In the oxidation process, Ge atoms are rejected form the SiO_2 layers, while out-diffusion of Ge atoms is suppressed by the oxide layers. As a result, the Ge fraction in the SiGe layer increases after the oxidation. It was reported that a strained SiGe-on-Insulator (SGOI) layer was obtained by oxidizing a thin SiGe layer on an SOI substrate[5]. By further oxidation of SGOI layer with adequate conditions of temperature and SiGe thickness, we have successfully fabricated ultra-thin strained GOI substrates.

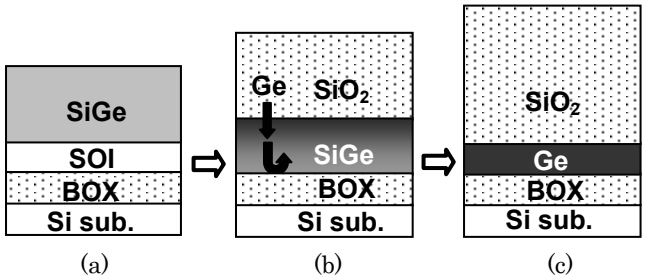

Fig. 1. Ge-on-Insulator fabrication process by Ge-condensation by oxidation technique. (a) SiGe is grown epitaxially on a SOI wafer, (b) Oxidation of SGOI, and (c) Ge is condensed completely.

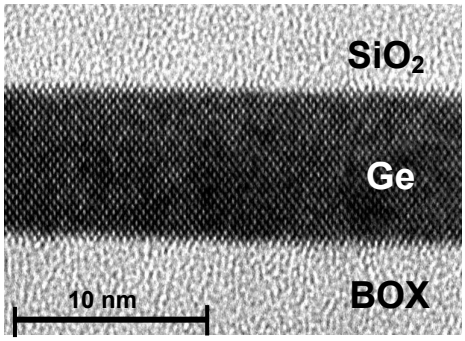

Fig. 2 Cross-sectional TEM image of a Strained GOI with Ge the layer thickness of 7 nm.

2. Fabrication and Characterization of GOI Structure

The process of GOI fabrication is schematically illustrated in Fig. 1. At first, a $Si_{1-x}Ge_x$ layer with a low Ge fraction (x = 0.15) was grown epitaxially by UHV-CVD on (100) surface of a commercially available bonded SOI wafer. Next, dry oxidation was carried out at temperatures lower than the melting temperatures of SiGe, which depends on Ge fraction. Finally, we obtained a thin GOI layer with the thickness lower than 10 nm. A cross-sectional TEM image of the fabricated GOI sample with the Ge thickness of 7 nm is presented in Fig. 2. As shown in the figure, the Ge layer exhibits good crystalline quality and smooth Ge/SiO_2 interfaces. The morphology of GOI surface was observed by AFM, which is presented in Fig. 3. In the figure, crosshatch pattern is observed. However, the surface exhibited a good roughness rms value of 0.4 nm estimated in 10 μm square. This rms value is much lower

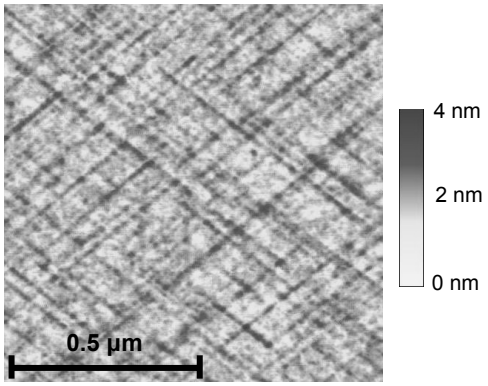

Fig. 3 AFM image of the GOI sample. The roughness of the surface is estimated to be ~0.42 nm as an rms value.

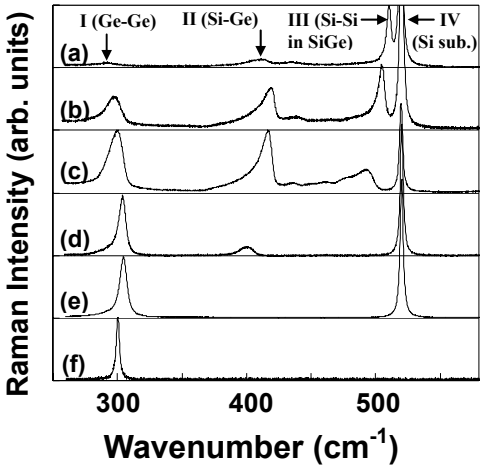

Fig. 4 Raman spectrum of SGOI layers of (a) x = 0.27, (b) x = 0.45, (c) x = 0.56, (d) x = 0.86, and (e) x = 1. Spectrum of unstrained bulk Ge (f) is also shown as a reference.

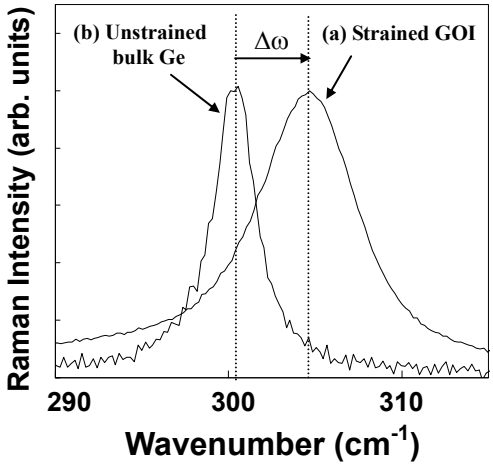

Fig. 5 Ge-Ge mode peaks in the Raman spectrum of strained GOI (a), and unstrained bulk Ge (b).

than the rms value (~5 nm) of a Ge layer grown directly on a thick SiGe buffer with Ge fraction up to 70%[6], and comparable to that after chemical mechanical polishing (CMP) process (~0.5 nm) [7].

Raman spectra were taken for SGOI layers of x = 0.27 (a), x = 0.45 (b), x = 0.56 (c), x = 0.86 (d), and x = 1 (e) after the Ge-condensation process. A spectrum of an unstrained bulk Ge (f) is also shown as a reference of the lattice relaxed Ge-Ge peak position. In the figure, the peaks labeled I, II, III and IV correspond to Ge-Ge mode, Si-Ge mode, Si-Si mode in the SiGe layer, and Si-Si mode in the substrate, respectively. Absence of Si in the GOI layer is evident from the disappearance of Si-Ge mode (II) and Si-Si mode (III) peaks in the Raman spectrum (e). It is estimated from the signal-to-noise ratio that the residual Si concentration in the GOI layer is less than 0.5%.

In order to reconfirm the absence of Si in the GOI layer directly, electron energy loss spectroscopy (EELS) measurement was also carried out. It has been found that no Si (less than 3%) was found in the GOI layer.

3. Strain in GOI layers

The strain in the Ge layer was evaluated from the Ge-Ge mode peak in the Raman spectra. Figure 5 represents the Ge-Ge mode peaks of the GOI samples and unstrained bulk Ge sample. Here, (a) and (b) are identical to that presented in Fig. 4 (e) and (f), respectively. The strain dependence of Raman shift in Ge, ω, is described as $\omega = \omega_{Ge} + 16\,\Sigma$ (cm^{-1}) [8] where ω_{Ge} is the Raman shift of relaxed Ge, and Σ is the normalized strain in Ge lattice. The normalized strain is defined as $\Sigma = \varepsilon / \varepsilon_0$, where ε is the strain in SiGe and ε_0 is the mismatch strain between relaxed Si and Ge, which is equal to 4.2%, therefore Σ = 0 for fully relaxed lattice and Σ = 1 for pseudomorphic Ge layer on relaxed Si. The difference of wavenumber between the strained Ge and the relaxed Ge, Δω, is 4.4 cm^{-1} as shown in Fig. 5, so we obtain Σ = 0.27 and then ε = 1.1%. This value of ε corresponds to that of a strained Ge layer pseudomorphically grown on a $Si_{1-x}Ge_x$ layer with x ~ 0.73, which is comparable to the reported value of the strained Ge layer on a thick SiGe buffer[3]. As a result, our ultra-thin strained GOI substrate is expected theoretically to exhibit the hole mobility ~8 times larger than that of unstrained Si[2].

In order to investigate the mechanism of relaxation of strain in the Ge layer to 1.1% from 4.2% for Ge on Si substrate, we evaluated the line density of dislocations from a plan-view TEM image. The obtained value of 18 μm^{-1} is much smaller than a theoretical value of 157 μm^{-1} which is based on the relaxation only by the misfit dislocations[9]. This means that the relaxation can not be explained only by dislocations, and the relaxation is enhanced by the increased viscosity of BOX, as similar with SGOI[10].

4. Summary

We have successfully fabricated ultra-thin (~10 nm) strained GOI substrates by oxidizing SiGe layers grown epitaxially on SOI wafers, which is applicable to 65 nm technology node and beyond. The purity of the GOI layer was estimated by Raman spectra and electron energy loss spectroscopy, and no residual Si (less than 0.5%) was detected. The surface morphology of the ultra-thin strained GOI layer was measured by AFM, and the rms value was found to be 0.4 nm, which is much smaller than that of a strained Ge surface on a thick SiGe buffer. The strain of the Ge layer was estimated to be 1.1% by Raman spectroscopy, which is enough for significant mobility enhancement.

Acknowledgement

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